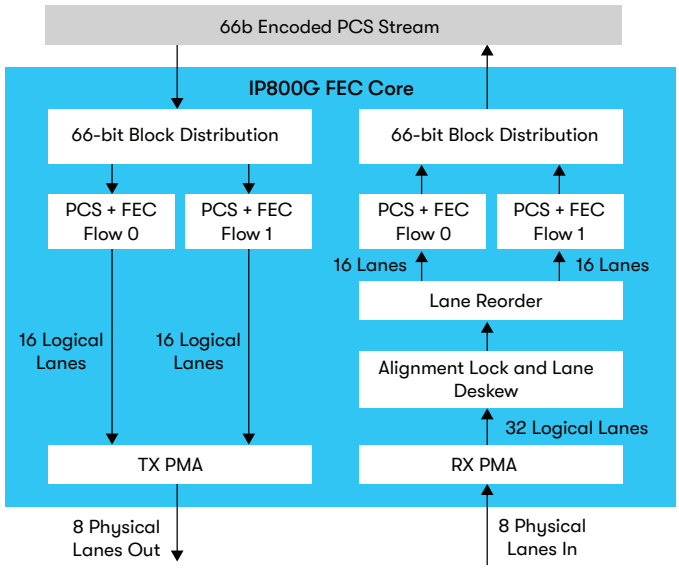
Product Brief

IP
Optical Transport, Ethernet LAN

FEC IP core for 800 Gbit/s Ethernet



Features

- Performs Reed-Solomon Forward Error Correction, RS-FEC (544,514,10)
- 256/257B transcoding, (de)scrambling
- Alignment Marker (AM) insertion / RX de-skewing, lane alignment. AM removal
- Performance monitoring and statistics:
  - Locking status for each of the logical lanes and aggregate alignment status
  - Corrected / Uncorrected FEC codeword count
  - Corrected FEC symbols and bit error counters per logical lane.
  - Symbol error rate (SER) threshold crossing status
  - AM signal fail status from peer
  - PCS 66b invalid sync header and type
- System side interface: 32 x 66 = 2112-bit data bus carrying 32 x 66b blocks of data
- Line side interface with 8 PMA interfaces of 4 x 256 bit for connecting to Agilex® 7 F-Tile FHT transceivers in PMA Direct mode
- Frequency of inner core logic >= 333 MHz (overspeed clock with data valid)

Product Family Supported

- Agilex® 7 F-Tile FHT transceivers

Description

The 800G EFEC IP core implements the IEEE 802.3 and Ethernet Technology Consortium (ETC) RS FEC encoder and decoder for transmission at 800 Gbit/s signal rates. This IP works seamlessly with the F-Tile FHT transceivers in Agilex® 7 FPGAs and SoCs when operating at 100 Gbit/s PAM4.

In the TX direction, a single 800 Gbit/s stream of 64B/66B encoded blocks is input to the RS-FEC. The 800G block stream is split into two 400G streams by round robin distribution of 64B/66B blocks towards two 400G RS-FEC cores (which in turn are based on two 200G RS-FEC cores) for transcoding, scrambling, FEC encoding, and AM insertion. Each 400G RS-FEC encoder produces streams of 10b FEC symbols, which are distributed over 16 FEC lanes @ 26.56 Gbit/s. All lanes are then bit multiplexed into 8 lanes connecting to the transceivers.

In the RX direction, 8 PMD bit lanes are received from the transceivers and bit-demultiplexed to 32 FEC lanes. De-skewing needs to take the skew of all 32 FEC lanes into consideration. Lane reordering looks at all 32 FEC lanes to be able to split the FEC lanes over the two 400 Gbit/s RS-FEC decoders for error correction, AM removal, de-scrambling, and reverse transcoding. A round robin 64B/66B block collector reconstructs the original 800 Gbit/s stream of 64B/66B encoded blocks.

Applications

- Optical Transport Networks
- Ethernet Local Area Networks

Ordering Information

- For ordering and discussion of specification details and options pls contact Altera or Altera Partner Zeuxion

Learn More

- Zeuxion on IP for Altera FPGAs and SoCs: Zeuxion ApS.
- For more information about Altera® FPGAs and SoCs or other products and solutions, visit altera.com.

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PB-1017-1.0