Pin Information for the Arria® II GZ EP2AGZ350 Device
Version 1.2
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
1A		TDI		TDI			H23	No			
1A		TMS		TMS			J21	No			
1A		TRST		TRST			G24	No			
1A		TCK		TCK			F24	No			
1A		TDO		TDO			H24	No			
1C	VREFB1CN0	IO		CLKUSR			M21	Yes			
1C	VREFB1CN0	IO		DATA0			N20	Yes			
1C	VREFB1CN0	IO		DATA1			M20	Yes			
1C	VREFB1CN0	IO		DATA2			L18	Yes			
1C	VREFB1CN0	IO		DATA3			K20	Yes			
1C	VREFB1CN0	IO		DATA4			M18	Yes			
1C	VREFB1CN0	IO		DATA5			M19	Yes			
1C	VREFB1CN0	IO		DATA6			L20	Yes			
1C	VREFB1CN0	IO		DATA7			N21	Yes			
1C	VREFB1CN0	IO		INIT_DONE			N18	Yes			
1C	VREFB1CN0	IO		CRC_ERROR			N19	Yes			
1C	VREFB1CN0	IO		DEV_OE			P20	Yes			
1C	VREFB1CN0	IO		DEV_CLRn			P19	Yes			
1C	VREFB1CN0	CLK1p	CLK1p				R20	No			
		nCONFIG		nCONFIG			U20	No			
		nSTATUS		nSTATUS			U21	No			
		CONF_DONE		CONF_DONE			V22	No			
		PORSEL					V19	No			
		nCE		nCE			V20	No			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AD23	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AD24	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AF23	Yes	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AE23	Yes	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AE24	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AF24	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AG26	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AF26	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AH26	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AH25	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AH24	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AG24	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AH22	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AH21	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH23	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AG23	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AG21	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AF21	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AF22	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AE22	Yes	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AC22	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AC21	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AE21	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AD21	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AB22	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	Y22	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AB23	Yes	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AA23	Yes	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	W22	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	Y21	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AA20	Yes	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	Y20	Yes	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AA21	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AB21	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AC20	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AB20	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	W20	Yes			
3A	VREFB3AN0	IO				DIFFOUT_B19p	W19	Yes			

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3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	Y19	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	Y18	Yes			
3C	VREFB3CN0	IO				DIFFOUT_B49n	AB18	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B49p	AB17	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B25n	DIFFOUT_B50n	AC19	Yes	DQSn17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B25p	DIFFOUT_B50p	AC18	Yes	DQS17B	DQ17B/CQn17B	
3C	VREFB3CN0	IO				DIFFOUT_B51n	AC17	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B51p	AA17	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	AE18	Yes	DQSn18B	DQSn17B/DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	AD18	Yes	DQS18B	DQS17B/CQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53n	AE20	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53p	AD17	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	AF19	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	AE19	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B55n	AG20	Yes	DQ19B		
3C	VREFB3CN0	IO				DIFFOUT_B55p	AH20	Yes	DQ19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B56n	AG18	Yes	DQSn19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B56p	AF18	Yes	DQS19B		
3C	VREFB3CN0	IO				DIFFOUT_B57n	AH19	Yes	DQ19B		
3C	VREFB3CN0	IO				DIFFOUT_B57p	AH18	Yes	DQ19B		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	Y17	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	Y16	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AA15	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	Y15	No			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AF15	No			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AE15	No			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AH17	No			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AH16	No			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AH15	No			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AG15	No			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AG14	No			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AH14	No			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AH12	No			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AH13	No			
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B34p	DIFFOUT_B67p	AE14	No			
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B34n	DIFFOUT_B67n	AF14	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B68p	Y14	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B68n	AA14	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AE13	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AF13	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B70p	AB13	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B70n	Y13	No			
4C	VREFB4CN0	IO				DIFFOUT_B72p	AH11	Yes	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B72n	AG11	Yes	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AG9	Yes	DQS20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AH9	Yes	DQSn20B		
4C	VREFB4CN0	IO				DIFFOUT_B74p	AF11	Yes	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B74n	AH10	Yes	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AD12	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AE12	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76p	AE9	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76n	AE11	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AE10	Yes	DQS21B	DQS22B/CQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AF10	Yes	DQSn21B	DQSn22B/DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78p	AC12	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78n	AB12	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AC11	Yes	DQS22B	DQ22B/CQn22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AD11	Yes	DQSn22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80p	AB11	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80n	AA11	Yes	DQ22B	DQ22B	
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	W11	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	W12	Yes			

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4A	VREFB4AN0	IO				DIFFOUT_B110p	Y10	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B110n	Y11	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AB10	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AC10	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112p	Y9	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112n	AA9	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AB9	Yes	DQS33B	DQS36B/CQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AC9	Yes	DQSn33B	DQSn36B/DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114p	Y8	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114n	AA8	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AB6	Yes	DQS34B	DQ36B/CQn36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AB7	Yes	DQSn34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116p	Y7	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116n	W8	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AD8	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	AE8	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118p	AC7	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AC8	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AE7	Yes	DQS35B	DQS37B/CQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	AF7	Yes	DQSn35B	DQSn37B/DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AF8	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	AG8	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AH6	Yes	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AH7	Yes	DQSn36B	DQ37B	DQSn38B/DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122p	AG6	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	AH8	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	AG5	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	AH5	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	AF4	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	AH4	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	AG3	Yes	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	AH3	Yes	DQSn37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	AF6	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	AE6	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	AE5	Yes	DQS38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	AF5	Yes	DQSn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	AD6	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	AC6	Yes	DQ38B	DQ38B	DQ38B
		nIO_PULLUP		nIO_PULLUP			AA5	No			
		nCEO		nCEO			V7	No			
		DCLK		DCLK			W7	No			
		nCSO		nCSO			U8	No			
		ASDO		ASDO			U9	No			
		MSEL2		MSEL2			N8	No			
		MSEL1		MSEL1			K7	No			
		MSEL0		MSEL0			N9	No			
7A	VREFB7AN0	IO				DIFFOUT_T1n	C3	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	C4	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A3	Yes	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	B3	Yes	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	A2	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B2	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	B5	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	C5	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	A5	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	A4	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	A6	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	B6	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	F6	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	F7	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	D6	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	E6	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T

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7A	VREFB7AN0	IO				DIFFOUT_T9n	D7	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	F8	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	C8	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	C7	Yes	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	A8	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	D8	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B8	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	J7	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	G8	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	G6	Yes	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	H6	Yes	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	K8	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	J8	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	J11	Yes	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	K10	Yes	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	J9	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	K9	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	H9	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	J10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	L9	Yes			
7A	VREFB7AN0	IO				DIFFOUT_T19p	M9	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	L10	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	M10	Yes			
7C	VREFB7CN0	IO				DIFFOUT_T49n	G9	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T49p	G11	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	F10	Yes	DQSn17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	G10	Yes	DQS17T	DQ17T/CQn17T	
7C	VREFB7CN0	IO				DIFFOUT_T51n	G12	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T51p	H11	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	E11	Yes	DQSn18T	DQSn17T/DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	F11	Yes	DQS18T	DQS17T/CQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53n	E12	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53p	F12	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	D9	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	E9	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T55n	B9	Yes	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T55p	C9	Yes	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	C10	Yes	DQSn19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	D10	Yes	DQS19T		
7C	VREFB7CN0	IO				DIFFOUT_T57n	D11	Yes	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T57p	C11	Yes	DQ19T		
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T59n	J13	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T59p	J12	No			
7C	VREFB7CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T60n	C13	No			
7C	VREFB7CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T60p	D13	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T61n	H14	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T61p	J14	No			
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T31n	DIFFOUT_T62n	A10	No			
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T31p	DIFFOUT_T62p	A9	No			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	A11	No			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	B11	No			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	A12	No			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	B12	No			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	B15	No			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	A15	No			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	A13	No			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	A14	No			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	C14	No			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	B14	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	J15	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	H15	No			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	D15	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	C15	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	J16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	G16	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	D16	Yes			
8C	VREFB8CN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	C16	Yes			
8C	VREFB8CN0	IO				DIFFOUT_T72p	A17	Yes	DQ20T		
8C	VREFB8CN0	IO				DIFFOUT_T72n	A16	Yes	DQ20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	C17	Yes	DQS20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	B17	Yes	DQSn20T		
8C	VREFB8CN0	IO				DIFFOUT_T74p	A18	Yes	DQ20T		
8C	VREFB8CN0	IO				DIFFOUT_T74n	D17	Yes	DQ20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	B18	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	A19	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76p	A20	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76n	B20	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	C19	Yes	DQS21T	DQS22T/CQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	C20	Yes	DQSn21T	DQSn22T/DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78p	F17	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78n	E17	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	D19	Yes	DQS22T	DQ22T/CQn22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	D18	Yes	DQSn22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80p	E18	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80n	F18	Yes	DQ22T	DQ22T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	J17	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	J18	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T110p	K18	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T110n	K19	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	E20	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	D20	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112p	F20	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112n	F21	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	E21	Yes	DQS33T	DQS36T/CQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	D21	Yes	DQSn33T	DQSn36T/DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114p	G19	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114n	G18	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	J20	Yes	DQS34T	DQ36T/CQn36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	H20	Yes	DQSn34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116p	H18	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116n	J19	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	B23	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	A22	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	B21	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118n	A21	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	B24	Yes	DQS35T	DQS37T/CQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	A23	Yes	DQSn35T	DQSn37T/DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	A25	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	A24	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	B26	Yes	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	A26	Yes	DQSn36T	DQ37T	DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	A27	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	B27	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	G21	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	F22	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	G22	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124n	G23	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	F23	Yes	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	E23	Yes	DQSn37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	C22	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	D22	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	D23	Yes	DQS38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	C23	Yes	DQSn38T	DQ38T	DQ38T

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
8A	VREFB8AN0	IO				DIFFOUT_T128p	C25	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	C24	Yes	DQ38T	DQ38T	DQ38T
QL1		GXB_TX_L7p					E25	No			
QL1		GXB_TX_L7n					E26	No			
QL1		GXB_RX_L7p					F27	No			
QL1		GXB_RX_L7n					F28	No			
QL1		GXB_TX_L6p					G25	No			
QL1		GXB_TX_L6n					G26	No			
QL1		GXB_RX_L6p					H27	No			
QL1		GXB_RX_L6n					H28	No			
QL1		REFCLK_L3p,GXB_CMURX_L3p					J25	No			
QL1		REFCLK_L3n,GXB_CMURX_L3n					J26	No			
QL1		REFCLK_L2p,GXB_CMURX_L2p					K27	No			
QL1		REFCLK_L2n,GXB_CMURX_L2n					K28	No			
QL1		GXB_TX_L5p					L25	No			
QL1		GXB_TX_L5n					L26	No			
QL1		GXB_RX_L5p					M27	No			
QL1		GXB_RX_L5n					M28	No			
QL1		GXB_TX_L4p					N25	No			
QL1		GXB_TX_L4n					N26	No			
QL1		GXB_RX_L4p					P27	No			
QL1		GXB_RX_L4n					P28	No			
QL0		GXB_TX_L3p					R25	No			
QL0		GXB_TX_L3n					R26	No			
QL0		GXB_RX_L3p					T27	No			
QL0		GXB_RX_L3n					T28	No			
QL0		GXB_TX_L2p					U25	No			
QL0		GXB_TX_L2n					U26	No			
QL0		GXB_RX_L2p					V27	No			
QL0		GXB_RX_L2n					V28	No			
QL0		REFCLK_L1p,GXB_CMURX_L1p					W25	No			
QL0		REFCLK_L1n,GXB_CMURX_L1n					W26	No			
QL0		REFCLK_L0p,GXB_CMURX_L0p					Y27	No			
QL0		REFCLK_L0n,GXB_CMURX_L0n					Y28	No			
QL0		GXB_TX_L1p					AA25	No			
QL0		GXB_TX_L1n					AA26	No			
QL0		GXB_RX_L1p					AB27	No			
QL0		GXB_RX_L1n					AB28	No			
QL0		GXB_TX_L0p					AC25	No			
QL0		GXB_TX_L0n					AC26	No			
QL0		GXB_RX_L0p					AD27	No			
QL0		GXB_RX_L0n					AD28	No			
QR0		GXB_RX_R0n					AD1	No			
QR0		GXB_RX_R0p					AD2	No			
QR0		GXB_TX_R0n					AC3	No			
QR0		GXB_TX_R0p					AC4	No			
QR0		GXB_RX_R1n					AB1	No			
QR0		GXB_RX_R1p					AB2	No			
QR0		GXB_TX_R1n					AA3	No			
QR0		GXB_TX_R1p					AA4	No			
QR0		REFCLK_R0n,GXB_CMURX_R0n					Y1	No			
QR0		REFCLK_R0p,GXB_CMURX_R0p					Y2	No			
QR0		REFCLK_R1n,GXB_CMURX_R1n					W3	No			
QR0		REFCLK_R1p,GXB_CMURX_R1p					W4	No			
QR0		GXB_RX_R2n					V1	No			
QR0		GXB_RX_R2p					V2	No			
QR0		GXB_TX_R2n					U3	No			
QR0		GXB_TX_R2p					U4	No			
QR0		GXB_RX_R3n					T1	No			
QR0		GXB_RX_R3p					T2	No			
QR0		GXB_TX_R3n					R3	No			
QR0		GXB_TX_R3p					R4	No			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
QR1		GXB_RX_R4n					P1	No			
QR1		GXB_RX_R4p					P2	No			
QR1		GXB_TX_R4n					N3	No			
QR1		GXB_TX_R4p					N4	No			
QR1		GXB_RX_R5n					M1	No			
QR1		GXB_RX_R5p					M2	No			
QR1		GXB_TX_R5n					L3	No			
QR1		GXB_TX_R5p					L4	No			
QR1		REFCLK_R2n,GXB_CMURX_R2n					K1	No			
QR1		REFCLK_R2p,GXB_CMURX_R2p					K2	No			
QR1		REFCLK_R3n,GXB_CMURX_R3n					J3	No			
QR1		REFCLK_R3p,GXB_CMURX_R3p					J4	No			
QR1		GXB_RX_R6n					H1	No			
QR1		GXB_RX_R6p					H2	No			
QR1		GXB_TX_R6n					G3	No			
QR1		GXB_TX_R6p					G4	No			
QR1		GXB_RX_R7n					F1	No			
QR1		GXB_RX_R7p					F2	No			
QR1		GXB_TX_R7n					E3	No			
QR1		GXB_TX_R7p					E4	No			
		GND					V9	No			
		GND					P14	No			
		GND					B28	No			
		GND					K16	No			
		GND					K14	No			
		GND					M12	No			
		GND					K12	No			
		GND					L11	No			
		GND					AH2	No			
		GND					AH27	No			
		GND					AG4	No			
		GND					AG7	No			
		GND					AG10	No			
		GND					AG13	No			
		GND					AG16	No			
		GND					AG19	No			
		GND					AG22	No			
		GND					AG25	No			
		GND					AD7	No			
		GND					AD10	No			
		GND					AD13	No			
		GND					AD16	No			
		GND					AD19	No			
		GND					AD22	No			
		GND					AA7	No			
		GND					AA10	No			
		GND					AA13	No			
		GND					AA16	No			
		GND					AA19	No			
		GND					AA22	No			
		GND					W13	No			
		GND					W15	No			
		GND					W17	No			
		GND					V8	No			
		GND					V10	No			
		GND					V12	No			
		GND					V14	No			
		GND					V16	No			
		GND					V18	No			
		GND					V21	No			
		GND					U11	No			
		GND					U13	No			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					U15	No			
		GND					U17	No			
		GND					T10	No			
		GND					T12	No			
		GND					T14	No			
		GND					T16	No			
		GND					T18	No			
		GND					R11	No			
		GND					R13	No			
		GND					R17	No			
		GND					P12	No			
		GND					P16	No			
		GND					P18	No			
		GND					N11	No			
		GND					N13	No			
		GND					N15	No			
		GND					N17	No			
		GND					M14	No			
		GND					M16	No			
		GND					L8	No			
		GND					L13	No			
		GND					L15	No			
		GND					L17	No			
		GND					L19	No			
		GND					L21	No			
		GND					H7	No			
		GND					H10	No			
		GND					H13	No			
		GND					H16	No			
		GND					H19	No			
		GND					H22	No			
		GND					E7	No			
		GND					E10	No			
		GND					E13	No			
		GND					E16	No			
		GND					E19	No			
		GND					E22	No			
		GND					B1	No			
		GND					B4	No			
		GND					B7	No			
		GND					B10	No			
		GND					B13	No			
		GND					B16	No			
		GND					B19	No			
		GND					B22	No			
		GND					B25	No			
		GND					AG17	No			
		GND					AF17	No			
		GND					AF16	No			
		GND					AE16	No			
		GND					AF12	No			
		GND					AG12	No			
		GND					C12	No			
		GND					D12	No			
		GND					G5	No			
		GND					H5	No			
		GND					C27	No			
		GND					AG27	No			
		GND					D27	No			
		GND					D26	No			
		GND					D25	No			
		GND					E28	No			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					E27	No			
		GND					F26	No			
		GND					F25	No			
		GND					G28	No			
		GND					G27	No			
		GND					H26	No			
		GND					H25	No			
		GND					J28	No			
		GND					J27	No			
		GND					J24	No			
		GND					K26	No			
		GND					K25	No			
		GND					K23	No			
		GND					L28	No			
		GND					L27	No			
		GND					L24	No			
		GND					M26	No			
		GND					M25	No			
		GND					M23	No			
		GND					N28	No			
		GND					N27	No			
		GND					N24	No			
		GND					P26	No			
		GND					C28	No			
		GND					AG28	No			
		GND					AF27	No			
		GND					AE27	No			
		GND					AE28	No			
		GND					AD25	No			
		GND					AD26	No			
		GND					AC27	No			
		GND					AC28	No			
		GND					AB25	No			
		GND					AB26	No			
		GND					AA27	No			
		GND					AA28	No			
		GND					Y23	No			
		GND					Y25	No			
		GND					Y26	No			
		GND					W24	No			
		GND					W27	No			
		GND					W28	No			
		GND					V23	No			
		GND					V25	No			
		GND					V26	No			
		GND					U24	No			
		GND					U27	No			
		GND					U28	No			
		GND					T23	No			
		GND					T25	No			
		GND					T26	No			
		GND					R24	No			
		GND					R27	No			
		GND					R28	No			
		GND					P23	No			
		GND					P25	No			
		GND					AG1	No			
		GND					C2	No			
		GND					D4	No			
		GND					D3	No			
		GND					D2	No			
		GND					E2	No			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					E1	No			
		GND					F4	No			
		GND					F3	No			
		GND					G2	No			
		GND					G1	No			
		GND					H4	No			
		GND					H3	No			
		GND					J5	No			
		GND					J2	No			
		GND					J1	No			
		GND					K6	No			
		GND					K4	No			
		GND					K3	No			
		GND					L5	No			
		GND					L2	No			
		GND					L1	No			
		GND					M6	No			
		GND					M4	No			
		GND					M3	No			
		GND					N5	No			
		GND					N2	No			
		GND					N1	No			
		GND					P6	No			
		GND					P4	No			
		GND					P3	No			
		GND					R5	No			
		GND					R2	No			
		GND					R1	No			
		GND					T6	No			
		GND					T4	No			
		GND					T3	No			
		GND					U5	No			
		GND					U2	No			
		GND					U1	No			
		GND					V6	No			
		GND					V4	No			
		GND					V3	No			
		GND					W5	No			
		GND					W2	No			
		GND					W1	No			
		GND					Y6	No			
		GND					Y4	No			
		GND					Y3	No			
		GND					AA2	No			
		GND					AA1	No			
		GND					AB4	No			
		GND					AB3	No			
		GND					AC2	No			
		GND					AC1	No			
		GND					AD4	No			
		GND					AD3	No			
		GND					AE2	No			
		GND					AE1	No			
		GND					AF2	No			
		GND					C1	No			
		GND					AG2	No			
		GND					P7	No			
		GND					R7	No			
		GND					N7	No			
		VCC					R14	No			
		VCC					V13	No			
		VCC					V15	No			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCC					U12	No			
		VCC					U14	No			
		VCC					U16	No			
		VCC					T11	No			
		VCC					T13	No			
		VCC					T15	No			
		VCC					T17	No			
		VCC					R10	No			
		VCC					R12	No			
		VCC					R16	No			
		VCC					R18	No			
		VCC					P11	No			
		VCC					P13	No			
		VCC					P15	No			
		VCC					P17	No			
		VCC					N12	No			
		VCC					N14	No			
		VCC					N16	No			
		VCC					M13	No			
		VCC					M15	No			
		VCC					L14	No			
		VCC					U10	No			
		VCC					V11	No			
		VCC					V17	No			
		VCC					U18	No			
		VCC					M11	No			
		VCC					M17	No			
		VCC					L12	No			
		VCC					L16	No			
		VCC					U22	No			
		VCC					T22	No			
		VCC					M22	No			
		VCC					L22	No			
		VCC					U7	No			
		VCC					T7	No			
		VCC					M7	No			
		VCC					L7	No			
		DNU					R15	No			
		VCCPGM					AA24	No			
		VCCPGM					AB5	No			
		VCC_CLKIN3C					AB15	No			
		VCC_CLKIN4C					AB14	No			
		VCC_CLKIN7C					G14	No			
		VCC_CLKIN8C					G15	No			
		VCCBAT					D5	No			
		VCCA_PLL_B1					AC16	No			
		VCCA_PLL_B2					AC13	No			
		VCCA_PLL_T1					F16	No			
		VCCA_PLL_T2					F13	No			
		VCCD_PLL_B1					AC15	No			
		VCCD_PLL_B2					AC14	No			
		VCCD_PLL_T1					F15	No			
		VCCD_PLL_T2					F14	No			
		VCCIO1C					K21	No			
		VCCIO3A					W21	No			
		VCCIO3A					AF25	No			
		VCCIO3A					AD20	No			
		VCCIO3A					AC23	No			
		VCCIO3C					AF20	No			
		VCCIO3C					AE17	No			
		VCCIO3C					AA18	No			
		VCCIO4A					AD9	No			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCCIO4A					AF3	No			
		VCCIO4A					AA6	No			
		VCCIO4A					W9	No			
		VCCIO4C					AD14	No			
		VCCIO4C					AF9	No			
		VCCIO4C					Y12	No			
		VCCIO7A					C6	No			
		VCCIO7A					M8	No			
		VCCIO7A					H8	No			
		VCCIO7A					E8	No			
		VCCIO7C					D14	No			
		VCCIO7C					H12	No			
		VCCIO7C					F9	No			
		VCCIO8A					C26	No			
		VCCIO8A					H21	No			
		VCCIO8A					F19	No			
		VCCIO8A					C21	No			
		VCCIO8C					C18	No			
		VCCIO8C					H17	No			
		VCCIO8C					E15	No			
		VCCPD1C					J22	No			
		VCCPD3A					W18	No			
		VCCPD3C					W16	No			
		VCCPD4A					W10	No			
		VCCPD4C					W14	No			
		VCCPD7A					K11	No			
		VCCPD7C					K13	No			
		VCCPD8A					K17	No			
		VCCPD8C					K15	No			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				K22	No			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB19	No			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AB16	No			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB8	No			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AA12	No			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G7	No			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G13	No			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G20	No			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G17	No			
		NC					D24	No			
		NC					T21	No			
		NC					R19	No			
		NC					AB24	No			
		NC					AC5	No			
		NC					P9	No			
		NC					F5	No			
		NC					AE25	No			
		NC					AE26	No			
		NC					AE3	No			
		NC					AE4	No			
		NC					U19	No			
		NC					T8	No			
		NC					T9	No			
		NC					T19	No			
		NC					T20	No			
		NC					R9	No			
		NC					P10	No			
		NC					N10	No			
		VCCAUX					E24	No			
		VCCAUX					AC24	No			
		VCCAUX					AD5	No			
		VCCAUX					E5	No			
		VCCA_L					N23	No			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCCA_L					R23	No			
		VCCA_R					R6	No			
		VCCA_R					N6	No			
		VCCH_GXBL0					V24	No			
		VCCH_GXBL1					L23	No			
		VCCH_GXBR0					V5	No			
		VCCH_GXBR1					L6	No			
		VCCL_GXBL0					W23	No			
		VCCL_GXBL0					Y24	No			
		VCCL_GXBL1					K24	No			
		VCCL_GXBL1					J23	No			
		VCCL_GXBR0					Y5	No			
		VCCL_GXBR0					W6	No			
		VCCL_GXBR1					K5	No			
		VCCL_GXBR1					J6	No			
		VCCR_L					U23	No			
		VCCR_L					M24	No			
		VCCR_R					M5	No			
		VCCR_R					U6	No			
		VCCT_L					T24	No			
		VCCT_L					P24	No			
		VCCT_R					P5	No			
		VCCT_R					T5	No			
		VCCHIP_L					N22	No			
		VCCHIP_L					R22	No			
		VCCHIP_L					P22	No			
		RREF_L0					AF28	No			
		RREF_L1					D28	No			
		RREF_R0					AF1	No			
		RREF_R1					D1	No			
		VCCCB					P21	No			
		VCCCB					R21	No			
		VCCCB					AD15	No			
		VCCCB					P8	No			
		VCCCB					R8	No			
		VCCCB					E14	No			

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the Arria II Device Family Pin Connection Guidelines.

(2) PLL_R1/R4 and PLL_L1/L4 outputs are not available in the EP2AGZ350 device.

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
1A		TDI		TDI			G28	No				
1A		TMS		TMS			H28	No				
1A		TRST		TRST			K26	No				
1A		TCK		TCK			F29	No				
1A		TDO		TDO			G29	No				
1A	VREFB1AN0	IO	PLL_L1_CLKOUT0n		DIFFIO_TX_L1n	DIFFOUT_L1n	G30	Yes				
1A	VREFB1AN0	IO	PLL_L1_FB_CLKOUT0p		DIFFIO_TX_L1p	DIFFOUT_L1p	H29	Yes				
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	E31	Yes				
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	E30	Yes				
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J29	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	J28	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	C32	Yes	DQSn1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	D32	Yes	DQS1L	DQ1L/CQn1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	K28	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	L27	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	B34	Yes	DQSn2L	DQSn1L/DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	A33	Yes	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	L26	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	M25	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	C34	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	B33	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	N25	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	N24	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	F32	Yes	DQSn3L	DQ2L	DQSn1L/DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	F31	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K29	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	L28	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	D34	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	D33	Yes	DQS4L	DQS2L/CQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	H31	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	H30	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	G32	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	G31	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	K30	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L29	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	E34	Yes	DQSn5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	E33	Yes	DQS5L	DQ3L/CQn3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	N27	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	N26	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	F34	Yes	DQSn6L	DQSn3L/DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	G33	Yes	DQS6L	DQS3L/CQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	K31	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	L30	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	J32	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	J31	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	M29	Yes	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	N28	Yes	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	G34	Yes	DQSn7L			
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	H33	Yes	DQS7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	P24	Yes	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	P23	Yes	DQ7L			
1C	VREFB1CN0	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	P26	Yes	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	R25	Yes	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L13n	DIFFOUT_L26n	K32	Yes	DQSn8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L13p	DIFFOUT_L26p	L31	Yes	DQS8L	DQ8L/CQn8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	N30	Yes	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	N29	Yes	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L14n	DIFFOUT_L28n	K34	Yes	DQSn9L	DQSn8L/DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L14p	DIFFOUT_L28p	K33	Yes	DQS9L	DQS8L/CQ8L	DQ8L/CQn8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L29n	P28	Yes	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	P27	Yes	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	L34	Yes	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	L33	Yes	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L31n	T25	Yes	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L31p	T24	Yes	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	M32	Yes	DQSn10L	DQ9L	DQSn8L/DQ8L	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
1C	VREFB1CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	M31	Yes	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	T23	Yes	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	U23	Yes	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	N32	Yes	DQSn11L	DQSn9L/DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	N31	Yes	DQS11L	DQS9L/CQ9L	DQ8L	
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	P29	Yes	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	R29	Yes	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	M34	Yes	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	N33	Yes	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	T29	Yes	DQ12L	DQ10L		
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	T28	Yes	DQ12L	DQ10L		
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	P32	Yes	DQSn12L	DQ10L		
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	P31	Yes	DQS12L	DQ10L/CQn10L		
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	T27	Yes	DQ12L	DQ10L		
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	T26	Yes	DQ12L	DQ10L		
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	N34	Yes	DQSn13L	DQSn10L/DQ10L		
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	P33	Yes	DQS13L	DQS10L/CQ10L		
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	V25	Yes	DQ13L	DQ10L		
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	U24	Yes	DQ13L	DQ10L		
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	R32	Yes	DQ13L	DQ10L		
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	R31	Yes	DQ13L	DQ10L		
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	V23	No				
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	W23	No				
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	T31	No				
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	T30	No				
1C	VREFB1CN0	CLK1n	CLK1n				P34	No				
1C	VREFB1CN0	CLK1p	CLK1p				R34	No				
		nCONFIG		nCONFIG			AC27	No				
		nSTATUS		nSTATUS			AM30	No				
		CONF_DONE		CONF_DONE			AN30	No				
		PORSEL					AL28	No				
		nCE		nCE			AM29	No				
3A	VREFB3AN0	IO				DIFFOUT_B1n	AA25	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AB25	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AC26	Yes	DQSn1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AC25	Yes	DQS1B	DQ1B/CQn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AB24	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AC24	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE25	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD26	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AD23	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AE24	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AE27	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AE26	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AG26	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AF24	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH27	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AH26	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AJ27	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AG25	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AH25	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AH24	Yes	DQS4B	DQS2B/CQ2B	DQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AJ25	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AK26	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AG23	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AF23	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AL27	Yes	DQ5B	DQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13p	AM27	Yes	DQ5B	DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AM26	Yes	DQSn5B	DQ3B		DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AL26	Yes	DQS5B	DQ3B/CQn3B		DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B15n	AK25	Yes	DQ5B	DQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B15p	AN28	Yes	DQ5B	DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AP32	Yes	DQSn6B	DQSn3B/DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AP31	Yes	DQS6B	DQS3B/CQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B17n	AP28	Yes	DQ6B	DQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B17p	AP27	Yes	DQ6B	DQ3B		DQ1B

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AP30	Yes	DQ6B	DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AP29	Yes	DQ6B	DQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B19n	AA23	Yes				DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B19p	AB23	Yes				DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AD22	Yes				DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AC22	Yes				DQ1B
3B	VREFB3BN0	IO				DIFFOUT_B25n	AC20	Yes	DQ9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B25p	AD20	Yes	DQ9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AF21	Yes	DQSn9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AE22	Yes	DQS9B	DQ9B/CQn9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B27n	AE20	Yes	DQ9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B27p	AE21	Yes	DQ9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AJ24	Yes	DQSn10B	DQSn9B/DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AH23	Yes	DQS10B	DQS9B/CQ9B	DQ9B/CQn9B	
3B	VREFB3BN0	IO				DIFFOUT_B29n	AG22	Yes	DQ10B	DQ9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B29p	AH21	Yes	DQ10B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AJ22	Yes	DQ10B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AH22	Yes	DQ10B	DQ9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B31n	AL23	Yes	DQ11B	DQ10B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B31p	AM23	Yes	DQ11B	DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AM24	Yes	DQSn11B	DQ10B	DQSn9B/DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AL24	Yes	DQS11B	DQ10B/CQn10B	DQS9B/CQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B33n	AK22	Yes	DQ11B	DQ10B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B33p	AK23	Yes	DQ11B	DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AP26	Yes	DQSn12B	DQSn10B/DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AN26	Yes	DQS12B	DQS10B/CQ10B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B35n	AM25	Yes	DQ12B	DQ10B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B35p	AP24	Yes	DQ12B	DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AP25	Yes	DQ12B	DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AN25	Yes	DQ12B	DQ10B	DQ9B	
3C	VREFB3CN0	IO				DIFFOUT_B49n	AM22	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B49p	AP22	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B25n	DIFFOUT_B50n	AP23	Yes	DQSn17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B25p	DIFFOUT_B50p	AN23	Yes	DQS17B	DQ17B/CQn17B		
3C	VREFB3CN0	IO				DIFFOUT_B51n	AP21	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B51p	AN22	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	AM21	Yes	DQSn18B	DQSn17B/DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	AL21	Yes	DQS18B	DQS17B/CQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B53n	AJ21	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B53p	AK20	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	AM20	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	AL20	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B55n	AN20	Yes	DQ19B			
3C	VREFB3CN0	IO				DIFFOUT_B55p	AJ20	Yes	DQ19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B56n	AM19	Yes	DQSn19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B56p	AL19	Yes	DQS19B			
3C	VREFB3CN0	IO				DIFFOUT_B57n	AK19	Yes	DQ19B			
3C	VREFB3CN0	IO				DIFFOUT_B57p	AJ19	Yes	DQ19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B58n	AH19	Yes				
3C	VREFB3CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B58p	AG19	Yes				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	AD19	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	AC18	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AE19	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	AE18	No				
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AM18	No				
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AL18	No				
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AP20	No				
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AP19	No				
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AP18	No				
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AP17	No				
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AP15	No				
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AP16	No				
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AM17	No				
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AN17	No				
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B34p	DIFFOUT_B67p	AK17	No				
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B34n	DIFFOUT_B67n	AL17	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B68p	AC16	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B68n	AD17	No				
4C	VREFB4CN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AE16	No				
4C	VREFB4CN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AF16	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B70p	AE15	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B70n	AD16	No				
4C	VREFB4CN0	IO				DIFFOUT_B72p	AJ16	Yes	DQ20B			
4C	VREFB4CN0	IO				DIFFOUT_B72n	AK16	Yes	DQ20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AM15	Yes	DQS20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AM16	Yes	DQSn20B			
4C	VREFB4CN0	IO				DIFFOUT_B74p	AL16	Yes	DQ20B			
4C	VREFB4CN0	IO				DIFFOUT_B74n	AH15	Yes	DQ20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AP13	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AP14	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B76p	AP12	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B76n	AN14	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AM13	Yes	DQS21B	DQS22B/CQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AN13	Yes	DQSn21B	DQSn22B/DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B78p	AL15	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B78n	AJ15	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AK14	Yes	DQS22B	DQ22B/CQn22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AL14	Yes	DQSn22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B80p	AJ14	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B80n	AM14	Yes	DQ22B	DQ22B		
4B	VREFB4BN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AJ13	Yes	DQ27B	DQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AK13	Yes	DQ27B	DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B94p	AG13	Yes	DQ27B	DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B94n	AH13	Yes	DQ27B	DQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B48p	DIFFOUT_B95p	AH12	Yes	DQS27B	DQS29B/CQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B48n	DIFFOUT_B95n	AJ12	Yes	DQSn27B	DQSn29B/DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B96p	AC14	Yes	DQ28B	DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B96n	AD14	Yes	DQ28B	DQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B49p	DIFFOUT_B97p	AF14	Yes	DQS28B	DQ29B/CQn29B	DQS30B/CQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B49n	DIFFOUT_B97n	AG14	Yes	DQSn28B	DQ29B	DQSn30B/DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B98p	AE14	Yes	DQ28B	DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B98n	AE13	Yes	DQ28B	DQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B50p	DIFFOUT_B99p	AM11	Yes	DQ29B	DQ30B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B50n	DIFFOUT_B99n	AN11	Yes	DQ29B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B100p	AL12	Yes	DQ29B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B100n	AM12	Yes	DQ29B	DQ30B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B51p	DIFFOUT_B101p	AK11	Yes	DQS29B	DQS30B/CQ30B	DQ30B/CQn30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B51n	DIFFOUT_B101n	AL11	Yes	DQSn29B	DQSn30B/DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B102p	AP11	Yes	DQ30B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B102n	AM10	Yes	DQ30B	DQ30B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B52p	DIFFOUT_B103p	AN10	Yes	DQS30B	DQ30B/CQn30B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B52n	DIFFOUT_B103n	AP10	Yes	DQSn30B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B104p	AP9	Yes	DQ30B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B104n	AM9	Yes	DQ30B	DQ30B	DQ30B	
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	Y12	Yes				DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	AA12	Yes				DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B110p	AC12	Yes				DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B110n	AD13	Yes				DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AP5	Yes	DQ33B	DQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AP6	Yes	DQ33B	DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B112p	AN7	Yes	DQ33B	DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B112n	AP7	Yes	DQ33B	DQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AP3	Yes	DQS33B	DQS36B/CQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AP4	Yes	DQSn33B	DQSn36B/DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B114p	AP8	Yes	DQ34B	DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B114n	AL9	Yes	DQ34B	DQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AM8	Yes	DQS34B	DQ36B/CQn36B		DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AN8	Yes	DQSn34B	DQ36B		DQSn38B/DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B116p	AL7	Yes	DQ34B	DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B116n	AL8	Yes	DQ34B	DQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AJ10	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	AK10	Yes	DQ35B	DQ37B	DQ38B	DQ38B

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
4A	VREFB4AN0	IO				DIFFOUT_B118p	AH11	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AJ11	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AF12	Yes	DQS35B	DQS37B/CQ37B	DQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	AG11	Yes	DQSn35B	DQSn37B/DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AJ9	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	AG10	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AJ8	Yes	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AK8	Yes	DQSn36B	DQ37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122p	AH8	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	AH9	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	AD9	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	AE9	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	AE11	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	AE12	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	AD11	Yes	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	AE10	Yes	DQSn37B	DQSn38B/DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	AB11	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	AB12	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	AB10	Yes	DQS38B	DQ38B/CQn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	AC10	Yes	DQSn38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	AA10	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	AA11	Yes	DQ38B	DQ38B	DQ38B	DQ38B
		nIO_PULLUP		nIO_PULLUP			AM6	No				
		nCEO		nCEO			AE8	No				
		DCLK		DCLK			AM5	No				
		nCSO		nCSO			AD8	No				
		ASDO		ASDO			AN5	No				
6C	VREFB6CN0	CLK10p	CLK10p				P1	No				
6C	VREFB6CN0	CLK10n	CLK10n				R1	No				
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	R3	No				
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	R2	No				
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	U12	No				
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	V12	No				
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	T5	Yes	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	T4	Yes	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	V11	Yes	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	U10	Yes	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	P4	Yes	DQS14R	DQS17R/CQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	P3	Yes	DQSn14R	DQSn17R/DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	T9	Yes	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	T8	Yes	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	N2	Yes	DQS15R	DQ17R/CQn17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	N1	Yes	DQSn15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	T11	Yes	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	T10	Yes	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	M2	Yes	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	M1	Yes	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	T7	Yes	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	T6	Yes	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	N4	Yes	DQS16R	DQS18R/CQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	N3	Yes	DQSn16R	DQSn18R/DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	R6	Yes	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	R5	Yes	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	K1	Yes	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R29n	DIFFOUT_R57n	L1	Yes	DQSn17R	DQ18R	DQSn19R/DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R29p	DIFFOUT_R58p	R12	Yes	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R29n	DIFFOUT_R58n	R11	Yes	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	K3	Yes	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	K2	Yes	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	R8	Yes	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	R7	Yes	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	L4	Yes	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R31n	DIFFOUT_R61n	L3	Yes	DQSn18R	DQSn19R/DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	P7	Yes	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	P6	Yes	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	M5	Yes	DQS19R	DQ19R/CQn19R	DQ19R	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
6C	VREFB6CN0	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	M4	Yes	DQSn19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	N6	Yes	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	N5	Yes	DQ19R	DQ19R	DQ19R	
6A	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	M7	Yes	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	M6	Yes	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	J4	Yes	DQS20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	J3	Yes	DQSn20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	P10	Yes	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	P9	Yes	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	G1	Yes	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R69n	H1	Yes	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	N9	Yes	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	N8	Yes	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	G2	Yes	DQS21R	DQS24R/CQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	F1	Yes	DQSn21R	DQSn24R/DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	L7	Yes	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	L6	Yes	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	H4	Yes	DQS22R	DQ24R/CQn24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	H3	Yes	DQSn22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	K6	Yes	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	K5	Yes	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	F2	Yes	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	E1	Yes	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	N11	Yes	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	N10	Yes	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	G4	Yes	DQS23R	DQS25R/CQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	G3	Yes	DQSn23R	DQSn25R/DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	N12	Yes	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	M11	Yes	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	D2	Yes	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	D1	Yes	DQSn24R	DQ25R	DQSn26R/DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	J6	Yes	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	J5	Yes	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	C2	Yes	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	C1	Yes	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	M9	Yes	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	M8	Yes	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	E4	Yes	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	E3	Yes	DQSn25R	DQSn26R/DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	K8	Yes	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	K7	Yes	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D4	Yes	DQS26R	DQ26R/CQn26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	D3	Yes	DQSn26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	F5	Yes	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	F4	Yes	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	A2	Yes				
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	B1	Yes				
6A	VREFB6AN0	IO	PLL_R1_FB_CLKOUT0p		DIFFIO_TX_R44p	DIFFOUT_R88p	H7	Yes				
6A	VREFB6AN0	IO	PLL_R1_CLKOUT0n		DIFFIO_TX_R44n	DIFFOUT_R88n	H6	Yes				
		MSEL2		MSEL2			K9	No				
		MSEL1		MSEL1			L10	No				
		MSEL0		MSEL0			J9	No				
7A	VREFB7AN0	IO				DIFFOUT_T1n	J11	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	K11	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	H12	Yes	DQSn1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	J12	Yes	DQS1T	DQ1T/CQn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	K12	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	L12	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	F8	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	G8	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	H9	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	G9	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	G10	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	H10	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	F7	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	F6	Yes	DQ3T	DQ2T	DQ1T	DQ1T

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	D6	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	E6	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	E7	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	D7	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	B4	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	C5	Yes	DQS4T	DQS2T/CQ2T	DQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	A5	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	A4	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A3	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B3	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	G11	Yes	DQ5T	DQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13p	E10	Yes	DQ5T	DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	Yes	DQSn5T	DQ3T		DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	Yes	DQS5T	DQ3T/CQn3T		DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T15n	E9	Yes	DQ5T	DQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T15p	F10	Yes	DQ5T	DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	A6	Yes	DQSn6T	DQSn3T/DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	B6	Yes	DQS6T	DQS3T/CQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T17n	A7	Yes	DQ6T	DQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T17p	C6	Yes	DQ6T	DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A8	Yes	DQ6T	DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B7	Yes	DQ6T	DQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T19n	L13	Yes				DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T19p	M13	Yes				DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	C9	Yes				DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	D9	Yes				DQ1T
7B	VREFB7BN0	IO				DIFFOUT_T25n	M15	Yes	DQ9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T25p	K13	Yes	DQ9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	J14	Yes	DQSn9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	K14	Yes	DQS9T	DQ9T/CQn9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T27n	K15	Yes	DQ9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T27p	L15	Yes	DQ9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	F13	Yes	DQSn10T	DQSn9T/DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	G13	Yes	DQS10T	DQS9T/CQ9T	DQ9T/CQn9T	
7B	VREFB7BN0	IO				DIFFOUT_T29n	G12	Yes	DQ10T	DQ9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T29p	H13	Yes	DQ10T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	F14	Yes	DQ10T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	G14	Yes	DQ10T	DQ9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T31n	D11	Yes	DQ11T	DQ10T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T31p	C11	Yes	DQ11T	DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	D12	Yes	DQSn11T	DQ10T	DQSn9T/DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	E12	Yes	DQS11T	DQ10T/CQn10T	DQS9T/CQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T33n	F11	Yes	DQ11T	DQ10T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T33p	E13	Yes	DQ11T	DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	A9	Yes	DQSn12T	DQSn10T/DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	B9	Yes	DQS12T	DQS10T/CQ10T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T35n	A11	Yes	DQ12T	DQ10T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T35p	C10	Yes	DQ12T	DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	A10	Yes	DQ12T	DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	B10	Yes	DQ12T	DQ10T	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T49n	A13	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T49p	A12	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	B13	Yes	DQSn17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	C13	Yes	DQS17T	DQ17T/CQn17T		
7C	VREFB7CN0	IO				DIFFOUT_T51n	C12	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T51p	B12	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	C14	Yes	DQSn18T	DQSn17T/DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	D14	Yes	DQS18T	DQS17T/CQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T53n	C15	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T53p	A14	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	A15	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	B15	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T55n	C16	Yes	DQ19T			
7C	VREFB7CN0	IO				DIFFOUT_T55p	D15	Yes	DQ19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	E15	Yes	DQSn19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	F15	Yes	DQS19T			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
7C	VREFB7CN0	IO				DIFFOUT_T57n	F16	Yes	DQ19T			
7C	VREFB7CN0	IO				DIFFOUT_T57p	E16	Yes	DQ19T			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T59n	M17	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T59p	L16	No				
7C	VREFB7CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T60n	H16	No				
7C	VREFB7CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T60p	J16	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T61n	K16	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T61p	K17	No				
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T31n	DIFFOUT_T62n	C17	No				
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T31p	DIFFOUT_T62p	D17	No				
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	A16	No				
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	B16	No				
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	A17	No				
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	A18	No				
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	C18	No				
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	B18	No				
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	A20	No				
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	A19	No				
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	E18	No				
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	D18	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	M19	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	L18	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	H19	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	G19	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	L19	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	K20	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	K19	Yes				
8C	VREFB8CN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	J19	Yes				
8C	VREFB8CN0	IO				DIFFOUT_T72p	F20	Yes	DQ20T			
8C	VREFB8CN0	IO				DIFFOUT_T72n	G20	Yes	DQ20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	E19	Yes	DQS20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	D19	Yes	DQSn20T			
8C	VREFB8CN0	IO				DIFFOUT_T74p	F19	Yes	DQ20T			
8C	VREFB8CN0	IO				DIFFOUT_T74n	C19	Yes	DQ20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	A23	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	A22	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T76p	B21	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T76n	A21	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	C22	Yes	DQS21T	DQS22T/CQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	B22	Yes	DQSn21T	DQSn22T/DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T78p	F21	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T78n	C20	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	E21	Yes	DQS22T	DQ22T/CQn22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	D21	Yes	DQSn22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T80p	D20	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T80n	C21	Yes	DQ22T	DQ22T		
8B	VREFB8BN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	A26	Yes	DQ27T	DQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	A25	Yes	DQ27T	DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T94p	A24	Yes	DQ27T	DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T94n	B24	Yes	DQ27T	DQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T95p	C26	Yes	DQS27T	DQS29T/CQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T95n	B25	Yes	DQSn27T	DQSn29T/DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T96p	E24	Yes	DQ28T	DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T96n	C25	Yes	DQ28T	DQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T49p	DIFFOUT_T97p	D24	Yes	DQS28T	DQ29T/CQn29T	DQS30T/CQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T49n	DIFFOUT_T97n	C24	Yes	DQSn28T	DQ29T	DQSn30T/DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T98p	D23	Yes	DQ28T	DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T98n	C23	Yes	DQ28T	DQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T50p	DIFFOUT_T99p	J21	Yes	DQ29T	DQ30T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T50n	DIFFOUT_T99n	H21	Yes	DQ29T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T100p	L21	Yes	DQ29T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T100n	M21	Yes	DQ29T	DQ30T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T51p	DIFFOUT_T101p	K22	Yes	DQS29T	DQS30T/CQ30T	DQ30T/CQn30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T51n	DIFFOUT_T101n	K21	Yes	DQSn29T	DQSn30T/DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T102p	E22	Yes	DQ30T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T102n	F22	Yes	DQ30T	DQ30T	DQ30T	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
8B	VREFB8BN0	IO			DIFFIO_RX_T52p	DIFFOUT_T103p	H22	Yes	DQS30T	DQ30T/CQn30T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T52n	DIFFOUT_T103n	G22	Yes	DQSn30T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T104p	F23	Yes	DQ30T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T104n	G23	Yes	DQ30T	DQ30T	DQ30T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	M23	Yes				DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	L22	Yes				DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T110p	L24	Yes				DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T110n	K25	Yes				DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	B28	Yes	DQ33T	DQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	A29	Yes	DQ33T	DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T112p	A27	Yes	DQ33T	DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T112n	A28	Yes	DQ33T	DQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	C27	Yes	DQS33T	DQS36T/CQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	B27	Yes	DQSn33T	DQSn36T/DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T114p	E25	Yes	DQ34T	DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T114n	F24	Yes	DQ34T	DQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	D26	Yes	DQS34T	DQ36T/CQn36T		DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	D27	Yes	DQSn34T	DQ36T		DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T116p	F25	Yes	DQ34T	DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T116n	E27	Yes	DQ34T	DQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	A31	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	A32	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	A30	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118n	B30	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	C31	Yes	DQS35T	DQS37T/CQ37T	DQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	B31	Yes	DQSn35T	DQSn37T/DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	E28	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	D28	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	D29	Yes	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	C29	Yes	DQSn36T	DQ37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	D30	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	C30	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	G26	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	F26	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	G25	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124n	H25	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	G27	Yes	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	F27	Yes	DQSn37T	DQSn38T/DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	J23	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	K23	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	J24	Yes	DQS38T	DQ38T/CQn38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	H24	Yes	DQSn38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128p	J25	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	K24	Yes	DQ38T	DQ38T	DQ38T	DQ38T
QL1		GXB_TX_L7p					V31	No				
QL1		GXB_TX_L7n					V32	No				
QL1		GXB_RX_L7p					U33	No				
QL1		GXB_RX_L7n					U34	No				
QL1		GXB_TX_L6p					Y31	No				
QL1		GXB_TX_L6n					Y32	No				
QL1		GXB_RX_L6p					W33	No				
QL1		GXB_RX_L6n					W34	No				
QL1		REFCLK_L3p,GXB_CMURX_L3p					AC29	No				
QL1		REFCLK_L3n,GXB_CMURX_L3n					AC30	No				
QL1		REFCLK_L2p,GXB_CMURX_L2p					AE29	No				
QL1		REFCLK_L2n,GXB_CMURX_L2n					AE30	No				
QL1		GXB_TX_L5p					AB31	No				
QL1		GXB_TX_L5n					AB32	No				
QL1		GXB_RX_L5p					AA33	No				
QL1		GXB_RX_L5n					AA34	No				
QL1		GXB_TX_L4p					AD31	No				
QL1		GXB_TX_L4n					AD32	No				
QL1		GXB_RX_L4p					AC33	No				
QL1		GXB_RX_L4n					AC34	No				
QL0		GXB_TX_L3p					AF31	No				
QL0		GXB_TX_L3n					AF32	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
QL0		GXB_RX_L3p					AE33	No				
QL0		GXB_RX_L3n					AE34	No				
QL0		GXB_TX_L2p					AH31	No				
QL0		GXB_TX_L2n					AH32	No				
QL0		GXB_RX_L2p					AG33	No				
QL0		GXB_RX_L2n					AG34	No				
QL0		REFCLK_L1p,GXB_CMURX_L1p					AG29	No				
QL0		REFCLK_L1n,GXB_CMURX_L1n					AG30	No				
QL0		REFCLK_L0p,GXB_CMURX_L0p					AJ29	No				
QL0		REFCLK_L0n,GXB_CMURX_L0n					AJ30	No				
QL0		GXB_TX_L1p					AK31	No				
QL0		GXB_TX_L1n					AK32	No				
QL0		GXB_RX_L1p					AJ33	No				
QL0		GXB_RX_L1n					AJ34	No				
QL0		GXB_TX_L0p					AM31	No				
QL0		GXB_TX_L0n					AM32	No				
QL0		GXB_RX_L0p					AL33	No				
QL0		GXB_RX_L0n					AL34	No				
QR0		GXB_RX_R0n					AL1	No				
QR0		GXB_RX_R0p					AL2	No				
QR0		GXB_TX_R0n					AM3	No				
QR0		GXB_TX_R0p					AM4	No				
QR0		GXB_RX_R1n					AJ1	No				
QR0		GXB_RX_R1p					AJ2	No				
QR0		GXB_TX_R1n					AK3	No				
QR0		GXB_TX_R1p					AK4	No				
QR0		REFCLK_R0n,GXB_CMURX_R0n					AJ5	No				
QR0		REFCLK_R0p,GXB_CMURX_R0p					AJ6	No				
QR0		REFCLK_R1n,GXB_CMURX_R1n					AG5	No				
QR0		REFCLK_R1p,GXB_CMURX_R1p					AG6	No				
QR0		GXB_RX_R2n					AG1	No				
QR0		GXB_RX_R2p					AG2	No				
QR0		GXB_TX_R2n					AH3	No				
QR0		GXB_TX_R2p					AH4	No				
QR0		GXB_RX_R3n					AE1	No				
QR0		GXB_RX_R3p					AE2	No				
QR0		GXB_TX_R3n					AF3	No				
QR0		GXB_TX_R3p					AF4	No				
QR1		GXB_RX_R4n					AC1	No				
QR1		GXB_RX_R4p					AC2	No				
QR1		GXB_TX_R4n					AD3	No				
QR1		GXB_TX_R4p					AD4	No				
QR1		GXB_RX_R5n					AA1	No				
QR1		GXB_RX_R5p					AA2	No				
QR1		GXB_TX_R5n					AB3	No				
QR1		GXB_TX_R5p					AB4	No				
QR1		REFCLK_R2n,GXB_CMURX_R2n					AE5	No				
QR1		REFCLK_R2p,GXB_CMURX_R2p					AE6	No				
QR1		REFCLK_R3n,GXB_CMURX_R3n					AC5	No				
QR1		REFCLK_R3p,GXB_CMURX_R3p					AC6	No				
QR1		GXB_RX_R6n					W1	No				
QR1		GXB_RX_R6p					W2	No				
QR1		GXB_TX_R6n					Y3	No				
QR1		GXB_TX_R6p					Y4	No				
QR1		GXB_RX_R7n					U1	No				
QR1		GXB_RX_R7p					U2	No				
QR1		GXB_TX_R7n					V3	No				
QR1		GXB_TX_R7p					V4	No				
		GND					AC8	No				
		GND					U18	No				
		GND					AN6	No				
		GND					AN9	No				
		GND					AN12	No				
		GND					AN15	No				
		GND					AN18	No				
		GND					AN21	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
		GND					AN24	No				
		GND					AN27	No				
		GND					AN29	No				
		GND					AK9	No				
		GND					AK12	No				
		GND					AK15	No				
		GND					AK18	No				
		GND					AK21	No				
		GND					AK24	No				
		GND					AK27	No				
		GND					AG9	No				
		GND					AG12	No				
		GND					AG15	No				
		GND					AG18	No				
		GND					AG21	No				
		GND					AG24	No				
		GND					AG27	No				
		GND					AF8	No				
		GND					AD12	No				
		GND					AD15	No				
		GND					AD18	No				
		GND					AD21	No				
		GND					AD24	No				
		GND					AD27	No				
		GND					AC9	No				
		GND					AC11	No				
		GND					AB13	No				
		GND					AB15	No				
		GND					AB17	No				
		GND					AB19	No				
		GND					AB21	No				
		GND					AA14	No				
		GND					AA16	No				
		GND					AA18	No				
		GND					AA20	No				
		GND					AA22	No				
		GND					AA24	No				
		GND					Y11	No				
		GND					Y13	No				
		GND					Y15	No				
		GND					Y17	No				
		GND					Y19	No				
		GND					Y21	No				
		GND					W14	No				
		GND					W16	No				
		GND					W18	No				
		GND					W20	No				
		GND					W22	No				
		GND					V13	No				
		GND					V15	No				
		GND					V19	No				
		GND					V21	No				
		GND					V24	No				
		GND					U11	No				
		GND					U14	No				
		GND					U16	No				
		GND					U20	No				
		GND					U22	No				
		GND					T13	No				
		GND					T15	No				
		GND					T17	No				
		GND					T19	No				
		GND					T21	No				
		GND					R14	No				
		GND					R16	No				
		GND					R18	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
		GND					R20	No				
		GND					R22	No				
		GND					R24	No				
		GND					R27	No				
		GND					R30	No				
		GND					R33	No				
		GND					P2	No				
		GND					P5	No				
		GND					P8	No				
		GND					P11	No				
		GND					P13	No				
		GND					P15	No				
		GND					P17	No				
		GND					P19	No				
		GND					P21	No				
		GND					N14	No				
		GND					N16	No				
		GND					N18	No				
		GND					N20	No				
		GND					N22	No				
		GND					M24	No				
		GND					M27	No				
		GND					M30	No				
		GND					M33	No				
		GND					L2	No				
		GND					L5	No				
		GND					L8	No				
		GND					L11	No				
		GND					L14	No				
		GND					L17	No				
		GND					L20	No				
		GND					L23	No				
		GND					J27	No				
		GND					J30	No				
		GND					J33	No				
		GND					H2	No				
		GND					H5	No				
		GND					H8	No				
		GND					H11	No				
		GND					H14	No				
		GND					H17	No				
		GND					H20	No				
		GND					H23	No				
		GND					H26	No				
		GND					F30	No				
		GND					F33	No				
		GND					E2	No				
		GND					E5	No				
		GND					E8	No				
		GND					E11	No				
		GND					E14	No				
		GND					E17	No				
		GND					E20	No				
		GND					E23	No				
		GND					E26	No				
		GND					E29	No				
		GND					C33	No				
		GND					B2	No				
		GND					B5	No				
		GND					B8	No				
		GND					B11	No				
		GND					B14	No				
		GND					B17	No				
		GND					B20	No				
		GND					B23	No				
		GND					B26	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
		GND					B29	No				
		GND					B32	No				
		GND					H34	No				
		GND					J34	No				
		GND					AG20	No				
		GND					AF19	No				
		GND					AG16	No				
		GND					AH16	No				
		GND					J2	No				
		GND					J1	No				
		GND					G16	No				
		GND					H15	No				
		GND					C3	No				
		GND					D5	No				
		GND					T34	No				
		GND					T33	No				
		GND					T32	No				
		GND					U32	No				
		GND					U31	No				
		GND					U29	No				
		GND					U27	No				
		GND					V34	No				
		GND					V33	No				
		GND					V30	No				
		GND					V28	No				
		GND					W32	No				
		GND					W31	No				
		GND					W29	No				
		GND					W27	No				
		GND					Y34	No				
		GND					Y33	No				
		GND					Y30	No				
		GND					Y28	No				
		GND					AA32	No				
		GND					AA31	No				
		GND					AA29	No				
		GND					AA27	No				
		GND					AB34	No				
		GND					AB33	No				
		GND					AB30	No				
		GND					AB28	No				
		GND					AC32	No				
		GND					AC31	No				
		GND					AD34	No				
		GND					AD33	No				
		GND					AD30	No				
		GND					AD29	No				
		GND					AE32	No				
		GND					AE31	No				
		GND					AF34	No				
		GND					AF33	No				
		GND					AF30	No				
		GND					AF29	No				
		GND					AG32	No				
		GND					AG31	No				
		GND					AP33	No				
		GND					AN31	No				
		GND					AN32	No				
		GND					AN33	No				
		GND					AM33	No				
		GND					AM34	No				
		GND					AL31	No				
		GND					AL32	No				
		GND					AK29	No				
		GND					AK30	No				
		GND					AK33	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
		GND					AK34	No				
		GND					AJ31	No				
		GND					AJ32	No				
		GND					AH29	No				
		GND					AH30	No				
		GND					AH33	No				
		GND					AH34	No				
		GND					T3	No				
		GND					T2	No				
		GND					T1	No				
		GND					U8	No				
		GND					U6	No				
		GND					U4	No				
		GND					U3	No				
		GND					V7	No				
		GND					V5	No				
		GND					V2	No				
		GND					V1	No				
		GND					W8	No				
		GND					W6	No				
		GND					W4	No				
		GND					W3	No				
		GND					Y7	No				
		GND					Y5	No				
		GND					Y2	No				
		GND					Y1	No				
		GND					AA8	No				
		GND					AA6	No				
		GND					AA4	No				
		GND					AA3	No				
		GND					AB7	No				
		GND					AB5	No				
		GND					AB2	No				
		GND					AB1	No				
		GND					AC4	No				
		GND					AC3	No				
		GND					AD6	No				
		GND					AD5	No				
		GND					AD2	No				
		GND					AD1	No				
		GND					AE4	No				
		GND					AE3	No				
		GND					AF6	No				
		GND					AF5	No				
		GND					AF2	No				
		GND					AF1	No				
		GND					AG4	No				
		GND					AG3	No				
		GND					AH6	No				
		GND					AH5	No				
		GND					AH2	No				
		GND					AH1	No				
		GND					AJ4	No				
		GND					AJ3	No				
		GND					AK6	No				
		GND					AK5	No				
		GND					AK2	No				
		GND					AK1	No				
		GND					AL4	No				
		GND					AL3	No				
		GND					AM2	No				
		GND					AM1	No				
		GND					AN4	No				
		GND					AN3	No				
		GND					AN2	No				
		GND					AP2	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
		GND					W9	No				
		GND					Y10	No				
		GND					Y9	No				
		VCC					U17	No				
		VCC					AB14	No				
		VCC					AB22	No				
		VCC					AA13	No				
		VCC					AA15	No				
		VCC					AA17	No				
		VCC					AA19	No				
		VCC					AA21	No				
		VCC					Y14	No				
		VCC					Y16	No				
		VCC					Y18	No				
		VCC					Y20	No				
		VCC					W15	No				
		VCC					W17	No				
		VCC					W19	No				
		VCC					W21	No				
		VCC					V14	No				
		VCC					V16	No				
		VCC					V18	No				
		VCC					V20	No				
		VCC					U15	No				
		VCC					U19	No				
		VCC					U21	No				
		VCC					T14	No				
		VCC					T16	No				
		VCC					T18	No				
		VCC					T20	No				
		VCC					R15	No				
		VCC					R17	No				
		VCC					R19	No				
		VCC					R21	No				
		VCC					P14	No				
		VCC					P16	No				
		VCC					P18	No				
		VCC					P20	No				
		VCC					P22	No				
		VCC					N13	No				
		VCC					N21	No				
		VCC					N19	No				
		VCC					AB16	No				
		VCC					AB18	No				
		VCC					AB20	No				
		VCC					Y22	No				
		VCC					W13	No				
		VCC					V22	No				
		VCC					U13	No				
		VCC					T22	No				
		VCC					R13	No				
		VCC					N15	No				
		VCC					N17	No				
		VCC					AB26	No				
		VCC					AB27	No				
		VCC					V26	No				
		VCC					U26	No				
		VCC					AB8	No				
		VCC					AB9	No				
		VCC					V9	No				
		VCC					U9	No				
		DNU					V17	No				
		VCCPGM					AD25	No				
		VCCPGM					AD10	No				
		VCC_CLKIN3C					AF18	No				
		VCC_CLKIN4C					AE17	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
		VCC_CLKIN7C					J17	No				
		VCC_CLKIN8C					K18	No				
		VCCBAT					G6	No				
		VCCA_PLL_B1					AJ18	No				
		VCCA_PLL_B2					AH17	No				
		VCCA_PLL_L2					W25	No				
		VCCA_PLL_R2					W10	No				
		VCCA_PLL_T1					G18	No				
		VCCA_PLL_T2					F17	No				
		VCCD_PLL_B1					AH18	No				
		VCCD_PLL_B2					AG17	No				
		VCCD_PLL_L2					W24	No				
		VCCD_PLL_R2					V10	No				
		VCCD_PLL_T1					H18	No				
		VCCD_PLL_T2					G17	No				
		VCCIO1A					P25	No				
		VCCIO1A					M28	No				
		VCCIO1A					K27	No				
		VCCIO1A					H32	No				
		VCCIO1A					E32	No				
		VCCIO1C					U25	No				
		VCCIO1C					R28	No				
		VCCIO1C					P30	No				
		VCCIO1C					L32	No				
		VCCIO3A					AM28	No				
		VCCIO3A					AJ26	No				
		VCCIO3A					AF25	No				
		VCCIO3A					AE23	No				
		VCCIO3B					AL25	No				
		VCCIO3B					AJ23	No				
		VCCIO3C					AN19	No				
		VCCIO3C					AL22	No				
		VCCIO3C					AH20	No				
		VCCIO4A					AM7	No				
		VCCIO4A					AH10	No				
		VCCIO4A					AF9	No				
		VCCIO4A					AF11	No				
		VCCIO4B					AL10	No				
		VCCIO4B					AL13	No				
		VCCIO4C					AN16	No				
		VCCIO4C					AJ17	No				
		VCCIO4C					AH14	No				
		VCCIO6A					L9	No				
		VCCIO6A					K4	No				
		VCCIO6A					J7	No				
		VCCIO6A					G5	No				
		VCCIO6A					F3	No				
		VCCIO6C					R4	No				
		VCCIO6C					R9	No				
		VCCIO6C					N7	No				
		VCCIO6C					M3	No				
		VCCIO7A					K10	No				
		VCCIO7A					F9	No				
		VCCIO7A					C4	No				
		VCCIO7A					C7	No				
		VCCIO7B					F12	No				
		VCCIO7B					D10	No				
		VCCIO7C					G15	No				
		VCCIO7C					D13	No				
		VCCIO7C					D16	No				
		VCCIO8A					L25	No				
		VCCIO8A					G24	No				
		VCCIO8A					F28	No				
		VCCIO8A					C28	No				
		VCCIO8B					D22	No				
		VCCIO8B					D25	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
		VCCIO8C					G21	No				
		VCCIO8C					F18	No				
		VCCIO8C					B19	No				
		VCCPD1A					N23	No				
		VCCPD1C					R23	No				
		VCCPD3A					AC23	No				
		VCCPD3B					AC21	No				
		VCCPD3C					AC19	No				
		VCCPD4A					AC13	No				
		VCCPD4B					AC15	No				
		VCCPD4C					AC17	No				
		VCCPD6A					P12	No				
		VCCPD6C					T12	No				
		VCCPD7A					M12	No				
		VCCPD7B					M14	No				
		VCCPD7C					M16	No				
		VCCPD8A					M22	No				
		VCCPD8B					M20	No				
		VCCPD8C					M18	No				
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				M26	No				
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				R26	No				
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AF26	No				
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AF22	No				
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AF20	No				
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AF10	No				
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AF13	No				
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AF15	No				
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				M10	No				
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				R10	No				
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				J10	No				
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				J13	No				
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				J15	No				
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				J26	No				
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				J22	No				
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				J20	No				
		NC					D31	No				
		NC					AK28	No				
		NC					AK7	No				
		NC					G7	No				
		NC					AL29	No				
		NC					AL30	No				
		NC					AL5	No				
		NC					AL6	No				
		NC					AJ7	No				
		NC					AJ28	No				
		NC					AH7	No				
		NC					AH28	No				
		NC					AG7	No				
		NC					AG28	No				
		NC					AF7	No				
		NC					AF28	No				
		NC					AE7	No				
		NC					AE28	No				
		NC					AD7	No				
		NC					AD28	No				
		NC					AC7	No				
		NC					AC28	No				
		VCCAUX					H27	No				
		VCCAUX					AF27	No				
		VCCAUX					AG8	No				
		VCCAUX					J8	No				
		VCCA_L					V29	No				
		VCCA_L					Y29	No				
		VCCA_R					V6	No				
		VCCA_R					Y6	No				
		VCCH_GXBL0					AA28	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152	DQS for X32/X36 for F1152 *(3)*
		VCCH_GXBL1					U28	No				
		VCCH_GXBR0					AA7	No				
		VCCH_GXBR1					U7	No				
		VCCL_GXBL0					Y27	No				
		VCCL_GXBL0					AA26	No				
		VCCL_GXBL1					V27	No				
		VCCL_GXBL1					W28	No				
		VCCL_GXBR0					AA9	No				
		VCCL_GXBR0					Y8	No				
		VCCL_GXBR1					V8	No				
		VCCL_GXBR1					W7	No				
		VCCR_L					U30	No				
		VCCR_L					AA30	No				
		VCCR_R					U5	No				
		VCCR_R					AA5	No				
		VCCT_L					W30	No				
		VCCT_L					AB29	No				
		VCCT_R					AB6	No				
		VCCT_R					W5	No				
		VCCHIP_L					W26	No				
		VCCHIP_L					Y26	No				
		VCCHIP_L					Y25	No				
		RREF_L0					AN34	No				
		RREF_R0					AN1	No				
		VCCCB					Y23	No				
		VCCCB					Y24	No				
		VCCCB					AF17	No				
		VCCCB					W11	No				
		VCCCB					W12	No				
		VCCCB					J18	No				

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the Arria II Device Family Pin Connection Guidelines.

(2) PLL_R1/R4 and PLL_L1/L4 outputs are not available in the EP2AGZ350 device.

(3) Altera's external memory interface IPs do not support placement of the BWSn pins outside the DQS/DQ group adjacent to the x32/x36 DQS/DQ groups where the write data pins reside. When using x32/x36 DQS/DQ groups that have 40 pins, BWSn inputs are not supported. However, if you are not using Altera's memory interface IPs and you are using x32/x36 DQS/DQ groups that have 40 pins, you can place the BWSn pins in a separate ×4 DQS/DQ group adjacent to the x32/x36 DQS/DQ group where the write data pins reside.

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
1A		TDI		TDI			J29	No				
1A		TMS		TMS			N27	No				
1A		TRST		TRST			A32	No				
1A		TCK		TCK			G30	No				
1A		TDO		TDO			F30	No				
1A	VREFB1AN0	IO	PLL_L1_CLKOUT0n		DIFFIO_TX_L1n	DIFFOUT_L1n	K29	Yes				
1A	VREFB1AN0	IO	PLL_L1_FB_CLKOUT0p		DIFFIO_TX_L1p	DIFFOUT_L1p	L29	Yes				
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C34	Yes				
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D34	Yes				
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J30	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	K30	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	C31	Yes	DQSn1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	D31	Yes	DQS1L	DQ1L/CQn1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	M28	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	N28	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	C35	Yes	DQSn2L	DQSn1L/DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	D35	Yes	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	H32	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J32	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	B32	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	C32	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M31	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	N31	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	C33	Yes	DQSn3L	DQ2L	DQSn1L/DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D33	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	M30	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	N30	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	G31	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	H31	Yes	DQS4L	DQS2L/CQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	M29	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	N29	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	E31	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	F31	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	K31	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L31	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	E32	Yes	DQSn5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	F32	Yes	DQS5L	DQ3L/CQn3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	R28	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	T28	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	E34	Yes	DQSn6L	DQSn3L/DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	F34	Yes	DQS6L	DQS3L/CQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	R27	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	T27	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	F35	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	G35	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	J33	Yes	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	K32	Yes	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	F33	Yes	DQSn7L			
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	G33	Yes	DQS7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	P29	Yes	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	R29	Yes	DQ7L			
1C	VREFB1CN0	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	L32	Yes	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	M32	Yes	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L13n	DIFFOUT_L26n	J35	Yes	DQSn8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L13p	DIFFOUT_L26p	J34	Yes	DQS8L	DQ8L/CQn8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	P32	Yes	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	P31	Yes	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L14n	DIFFOUT_L28n	K35	Yes	DQSn9L	DQSn8L/DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L14p	DIFFOUT_L28p	K34	Yes	DQS9L	DQS8L/CQ8L	DQ8L/CQn8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L29n	T31	Yes	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	T30	Yes	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	N34	Yes	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	N33	Yes	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L31n	R33	Yes	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L31p	R32	Yes	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	M34	Yes	DQSn10L	DQ9L	DQSn8L/DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	M33	Yes	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	V28	Yes	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	W28	Yes	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	L35	Yes	DQSn11L	DQSn9L/DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	L34	Yes	DQS11L	DQS9L/CQ9L	DQ8L	
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	R31	Yes	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	R30	Yes	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	V31	Yes	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	U31	Yes	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	W30	Yes	DQ12L	DQ10L		
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	W29	Yes	DQ12L	DQ10L		
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	N35	Yes	DQSn12L	DQ10L		
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	P34	Yes	DQS12L	DQ10L/CQn10L		
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	V27	Yes	DQ12L	DQ10L		
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	W26	Yes	DQ12L	DQ10L		
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	R35	Yes	DQSn13L	DQSn10L/DQ10L		
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	R34	Yes	DQS13L	DQS10L/CQ10L		
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	V30	Yes	DQ13L	DQ10L		
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	V29	Yes	DQ13L	DQ10L		
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	U35	Yes	DQ13L	DQ10L		
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	V34	Yes	DQ13L	DQ10L		
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	W33	No				
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	W32	No				
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	W35	No				
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	W34	No				
1C	VREFB1CN0	CLK1n	CLK1n				AA35	No				
1C	VREFB1CN0	CLK1p	CLK1p				AB34	No				
2C	VREFB2CN0	CLK3p	CLK3p				AC34	No				
2C	VREFB2CN0	CLK3n	CLK3n				AC35	No				
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L23p	DIFFOUT_L45p	AF34	No				
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L23n	DIFFOUT_L45n	AE35	No				
2C	VREFB2CN0	IO	PLL_L3_FB_CLKOUT0p		DIFFIO_TX_L23p	DIFFOUT_L46p	AG34	No				
2C	VREFB2CN0	IO	PLL_L3_CLKOUT0n		DIFFIO_TX_L23n	DIFFOUT_L46n	AG35	No				
2C	VREFB2CN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AC31	Yes	DQ14L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AC32	Yes	DQ14L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	AB30	Yes	DQ14L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	AB31	Yes	DQ14L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AJ34	Yes	DQS14L	DQS17L/CQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AJ35	Yes	DQSn14L	DQSn17L/DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AB27	Yes	DQ15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AB28	Yes	DQ15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AH34	Yes	DQS15L	DQ17L/CQn17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AH35	Yes	DQSn15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	AC28	Yes	DQ15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	AC29	Yes	DQ15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AK34	Yes	DQ16L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AK35	Yes	DQ16L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	AG31	Yes	DQ16L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AG32	Yes	DQ16L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	AL34	Yes	DQS16L	DQS18L/CQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L28n	DIFFOUT_L55n	AL35	Yes	DQSn16L	DQSn18L/DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AD28	Yes	DQ17L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AD29	Yes	DQ17L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L29p	DIFFOUT_L57p	AH32	Yes	DQS17L	DQ18L/CQn18L	DQS19L/CQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L29n	DIFFOUT_L57n	AH33	Yes	DQSn17L	DQ18L	DQSn19L/DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L29p	DIFFOUT_L58p	AE28	Yes	DQ17L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L29n	DIFFOUT_L58n	AE29	Yes	DQ17L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L30p	DIFFOUT_L59p	AN34	Yes	DQ18L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L30n	DIFFOUT_L59n	AN35	Yes	DQ18L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L30p	DIFFOUT_L60p	AD30	Yes	DQ18L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L30n	DIFFOUT_L60n	AD31	Yes	DQ18L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L31p	DIFFOUT_L61p	AM34	Yes	DQS18L	DQS19L/CQ19L	DQ19L/CQn19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L31n	DIFFOUT_L61n	AM35	Yes	DQSn18L	DQSn19L/DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L31p	DIFFOUT_L62p	AF29	Yes	DQ19L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L31n	DIFFOUT_L62n	AG30	Yes	DQ19L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L32p	DIFFOUT_L63p	AJ32	Yes	DQS19L	DQ19L/CQn19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L32n	DIFFOUT_L63n	AK33	Yes	DQSn19L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L32p	DIFFOUT_L64p	AE30	Yes	DQ19L	DQ19L	DQ19L	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
2C	VREFB2CN0	IO			DIFFIO_TX_L32n	DIFFOUT_L64n	AE31	Yes	DQ19L	DQ19L	DQ19L	
2A	VREFB2AN0	IO			DIFFIO_RX_L33p	DIFFOUT_L65p	AN32	Yes				
2A	VREFB2AN0	IO			DIFFIO_RX_L33n	DIFFOUT_L65n	AP33	Yes				
2A	VREFB2AN0	IO			DIFFIO_TX_L33p	DIFFOUT_L66p	AC26	Yes	DQ20L			
2A	VREFB2AN0	IO			DIFFIO_TX_L33n	DIFFOUT_L66n	AD26	Yes	DQ20L			
2A	VREFB2AN0	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AN33	Yes	DQS20L			
2A	VREFB2AN0	IO			DIFFIO_RX_L34n	DIFFOUT_L67n	AP34	Yes	DQSn20L			
2A	VREFB2AN0	IO			DIFFIO_TX_L34p	DIFFOUT_L68p	AD27	Yes	DQ20L			
2A	VREFB2AN0	IO			DIFFIO_TX_L34n	DIFFOUT_L68n	AE27	Yes	DQ20L			
2A	VREFB2AN0	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AT34	Yes	DQ21L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AR34	Yes	DQ21L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AJ31	Yes	DQ21L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L35n	DIFFOUT_L70n	AH30	Yes	DQ21L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AT33	Yes	DQS21L	DQS24L/CQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L36n	DIFFOUT_L71n	AU33	Yes	DQSn21L	DQSn24L/DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L36p	DIFFOUT_L72p	AK32	Yes	DQ22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L36n	DIFFOUT_L72n	AL32	Yes	DQ22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AP35	Yes	DQS22L	DQ24L/CQn24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	AR35	Yes	DQSn22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AG29	Yes	DQ22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AH29	Yes	DQ22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AP32	Yes	DQ23L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AR32	Yes	DQ23L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AK31	Yes	DQ23L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	AL31	Yes	DQ23L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	AN30	Yes	DQS23L	DQS25L/CQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	AP30	Yes	DQSn23L	DQSn25L/DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	AE26	Yes	DQ24L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	AF26	Yes	DQ24L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AM31	Yes	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AN31	Yes	DQSn24L	DQ25L	DQSn26L/DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AK30	Yes	DQ24L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AL30	Yes	DQ24L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AT31	Yes	DQ25L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AU31	Yes	DQ25L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AG28	Yes	DQ25L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AH28	Yes	DQ25L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AR31	Yes	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AT30	Yes	DQSn25L	DQSn26L/DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	AG27	Yes	DQ26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	AH27	Yes	DQ26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AT32	Yes	DQS26L	DQ26L/CQn26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AU32	Yes	DQSn26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	AL29	Yes	DQ26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AM29	Yes	DQ26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AU34	Yes				
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AV34	Yes				
2A	VREFB2AN0	IO	PLL_L4_FB_CLKOUT0p		DIFFIO_TX_L44p	DIFFOUT_L88p	AJ29	Yes				
2A	VREFB2AN0	IO	PLL_L4_CLKOUT0n		DIFFIO_TX_L44n	DIFFOUT_L88n	AK29	Yes				
		nCONFIG		nCONFIG			AW36	No				
		nSTATUS		nSTATUS			AW35	No				
		CONF_DONE		CONF_DONE			AV35	No				
		PORSEL					AP29	No				
		nCE		nCE			AN29	No				
3A	VREFB3AN0	IO				DIFFOUT_B1n	AD25	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AE25	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AG25	Yes	DQSn1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AF25	Yes	DQS1B	DQ1B/CQn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AE24	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AK27	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AK26	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AJ26	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AH26	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AL27	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AK25	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AJ25	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AW34	Yes	DQ3B	DQ2B	DQ1B	DQ1B

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
3A	VREFB3AN0	IO				DIFFOUT_B7p	AW33	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AW32	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AV32	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AV31	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AW31	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AW30	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AV29	Yes	DQS4B	DQS2B/CQ2B	DQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AW28	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AW27	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AW29	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AV28	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AN27	Yes	DQ5B	DQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13p	AP27	Yes	DQ5B	DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AN26	Yes	DQSn5B	DQ3B		DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AM26	Yes	DQS5B	DQ3B/CQn3B		DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B15n	AP26	Yes	DQ5B	DQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B15p	AL25	Yes	DQ5B	DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AR28	Yes	DQSn6B	DQSn3B/DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AP28	Yes	DQS6B	DQS3B/CQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B17n	AT29	Yes	DQ6B	DQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B17p	AU29	Yes	DQ6B	DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AU28	Yes	DQ6B	DQ3B		DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AT28	Yes	DQ6B	DQ3B		DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B19n	AG24	Yes				DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B19p	AH24	Yes				DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AU27	Yes				DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AT27	Yes				DQ1B
3B	VREFB3BN0	IO				DIFFOUT_B25n	AM25	Yes	DQ9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B25p	AN25	Yes	DQ9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AP24	Yes	DQSn9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AN24	Yes	DQS9B	DQ9B/CQn9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B27n	AP25	Yes	DQ9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B27p	AR25	Yes	DQ9B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AU26	Yes	DQSn10B	DQSn9B/DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AT26	Yes	DQS10B	DQS9B/CQ9B	DQ9B/CQn9B	
3B	VREFB3BN0	IO				DIFFOUT_B29n	AT25	Yes	DQ10B	DQ9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B29p	AU25	Yes	DQ10B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AW26	Yes	DQ10B	DQ9B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AV26	Yes	DQ10B	DQ9B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B31n	AH22	Yes	DQ11B	DQ10B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B31p	AE23	Yes	DQ11B	DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AG22	Yes	DQSn11B	DQ10B	DQSn9B/DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AF22	Yes	DQS11B	DQ10B/CQn10B	DQS9B/CQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B33n	AE22	Yes	DQ11B	DQ10B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B33p	AF23	Yes	DQ11B	DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AL23	Yes	DQSn12B	DQSn10B/DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AK23	Yes	DQS12B	DQS10B/CQ10B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B35n	AK24	Yes	DQ12B	DQ10B	DQ9B	
3B	VREFB3BN0	IO				DIFFOUT_B35p	AJ22	Yes	DQ12B	DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AJ23	Yes	DQ12B	DQ10B	DQ9B	
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AH23	Yes	DQ12B	DQ10B	DQ9B	
3C	VREFB3CN0	IO				DIFFOUT_B49n	AN23	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B49p	AM23	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B25n	DIFFOUT_B50n	AN22	Yes	DQSn17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B25p	DIFFOUT_B50p	AM22	Yes	DQS17B	DQ17B/CQn17B		
3C	VREFB3CN0	IO				DIFFOUT_B51n	AL21	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B51p	AL22	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	AU24	Yes	DQSn18B	DQSn17B/DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	AT24	Yes	DQS18B	DQS17B/CQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B53n	AR23	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B53p	AP23	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	AU23	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	AT23	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B55n	AG20	Yes	DQ19B			
3C	VREFB3CN0	IO				DIFFOUT_B55p	AD21	Yes	DQ19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B56n	AF20	Yes	DQSn19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B56p	AE20	Yes	DQS19B			

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
3C	VREFB3CN0	IO				DIFFOUT_B57n	AE21	Yes	DQ19B			
3C	VREFB3CN0	IO				DIFFOUT_B57p	AG21	Yes	DQ19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B58n	AW25	Yes				
3C	VREFB3CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B58p	AV25	Yes				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	AJ20	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	AH20	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AP21	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	AN21	No				
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AU22	No				
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AT22	No				
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AW22	No				
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AV22	No				
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AT21	No				
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AR22	No				
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AW20	No				
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AW21	No				
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AV19	No				
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AW19	No				
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B34p	DIFFOUT_B67p	AR20	No				
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B34n	DIFFOUT_B67n	AT20	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B68p	AN20	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B68n	AP20	No				
4C	VREFB4CN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AU20	No				
4C	VREFB4CN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AV20	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B70p	AH18	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B70n	AH19	No				
4C	VREFB4CN0	IO				DIFFOUT_B72p	AD19	Yes	DQ20B			
4C	VREFB4CN0	IO				DIFFOUT_B72n	AG19	Yes	DQ20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AE19	Yes	DQS20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AF19	Yes	DQSn20B			
4C	VREFB4CN0	IO				DIFFOUT_B74p	AG18	Yes	DQ20B			
4C	VREFB4CN0	IO				DIFFOUT_B74n	AE18	Yes	DQ20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AT18	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AU18	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B76p	AT17	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B76n	AW18	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AU17	Yes	DQS21B	DQS22B/CQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AV17	Yes	DQSn21B	DQSn22B/DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B78p	AN19	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B78n	AM19	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AN18	Yes	DQS22B	DQ22B/CQn22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AP18	Yes	DQSn22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B80p	AR19	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B80n	AP19	Yes	DQ22B	DQ22B		
4B	VREFB4BN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AK17	Yes	DQ27B	DQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AL17	Yes	DQ27B	DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B94p	AJ16	Yes	DQ27B	DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B94n	AM17	Yes	DQ27B	DQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B48p	DIFFOUT_B95p	AK16	Yes	DQS27B	DQS29B/CQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B48n	DIFFOUT_B95n	AL16	Yes	DQSn27B	DQSn29B/DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B96p	AH17	Yes	DQ28B	DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B96n	AE17	Yes	DQ28B	DQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B49p	DIFFOUT_B97p	AF17	Yes	DQS28B	DQ29B/CQn29B	DQS30B/CQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B49n	DIFFOUT_B97n	AG17	Yes	DQSn28B	DQ29B	DQSn30B/DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B98p	AH16	Yes	DQ28B	DQ29B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B98n	AG16	Yes	DQ28B	DQ29B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B50p	DIFFOUT_B99p	AP17	Yes	DQ29B	DQ30B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B50n	DIFFOUT_B99n	AR17	Yes	DQ29B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B100p	AN16	Yes	DQ29B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B100n	AN17	Yes	DQ29B	DQ30B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B51p	DIFFOUT_B101p	AP16	Yes	DQS29B	DQS30B/CQ30B	DQ30B/CQn30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B51n	DIFFOUT_B101n	AR16	Yes	DQSn29B	DQSn30B/DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B102p	AW16	Yes	DQ30B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B102n	AT16	Yes	DQ30B	DQ30B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B52p	DIFFOUT_B103p	AU16	Yes	DQS30B	DQ30B/CQn30B	DQ30B	
4B	VREFB4BN0	IO			DIFFIO_RX_B52n	DIFFOUT_B103n	AV16	Yes	DQSn30B	DQ30B	DQ30B	
4B	VREFB4BN0	IO				DIFFOUT_B104p	AU15	Yes	DQ30B	DQ30B	DQ30B	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
4B	VREFB4BN0	IO				DIFFOUT_B104n	AT15	Yes	DQ30B	DQ30B	DQ30B	
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	AN15	Yes				DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	AP15	Yes				DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B110p	AE16	Yes				DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B110n	AF16	Yes				DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AV14	Yes	DQ33B	DQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AW14	Yes	DQ33B	DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B112p	AT14	Yes	DQ33B	DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B112n	AU14	Yes	DQ33B	DQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AV13	Yes	DQS33B	DQS36B/CQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AW13	Yes	DQSn33B	DQSn36B/DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B114p	AW12	Yes	DQ34B	DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B114n	AW11	Yes	DQ34B	DQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AU11	Yes	DQS34B	DQ36B/CQn36B		DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AV11	Yes	DQSn34B	DQ36B		DQSn38B/DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B116p	AT12	Yes	DQ34B	DQ36B		DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B116n	AU12	Yes	DQ34B	DQ36B		DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AP14	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	AR14	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118p	AP13	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AN14	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AR13	Yes	DQS35B	DQS37B/CQ37B	DQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	AT13	Yes	DQSn35B	DQSn37B/DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AN13	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	AL15	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AL13	Yes	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AM13	Yes	DQSn36B	DQ37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122p	AL14	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	AM14	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	AJ13	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	AK13	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	AH13	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	AK14	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	AH14	Yes	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	AJ14	Yes	DQSn37B	DQSn38B/DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	AG14	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	AG15	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	AE14	Yes	DQS38B	DQ38B/CQn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	AF14	Yes	DQSn38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	AD15	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	AE15	Yes	DQ38B	DQ38B	DQ38B	DQ38B
		nIO_PULLUP		nIO_PULLUP			AM11	No				
		nCEO		nCEO			AT11	No				
		DCLK		DCLK			AR11	No				
		nCSO		nCSO			AP11	No				
		ASDO		ASDO			AN11	No				
5A	VREFB5AN0	IO	PLL_R4_CLKOUT0n		DIFFIO_TX_R1n	DIFFOUT_R1n	AM10	Yes				
5A	VREFB5AN0	IO	PLL_R4_FB_CLKOUT0p		DIFFIO_TX_R1p	DIFFOUT_R1p	AL10	Yes				
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AW7	Yes				
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AV7	Yes				
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AP10	Yes	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AN10	Yes	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AW8	Yes	DQSn1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AV8	Yes	DQS1R	DQ1R/CQn1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AJ11	Yes	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AH11	Yes	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AU10	Yes	DQSn2R	DQSn1R/DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AT10	Yes	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AH12	Yes	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AG12	Yes	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AW10	Yes	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AV10	Yes	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AG13	Yes	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AF13	Yes	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AU9	Yes	DQSn3R	DQ2R	DQSn1R/DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AT9	Yes	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AP9	Yes	DQ3R	DQ2R	DQ1R	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AN9	Yes	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AU8	Yes	DQSn4R	DQSn2R/DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AT8	Yes	DQS4R	DQS2R/CQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AP7	Yes	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AN7	Yes	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AR8	Yes	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AP8	Yes	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AL9	Yes	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AK9	Yes	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AU7	Yes	DQSn5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AT7	Yes	DQS5R	DQ3R/CQn3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AM8	Yes	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AL8	Yes	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AU6	Yes	DQSn6R	DQSn3R/DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AT6	Yes	DQS6R	DQS3R/CQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AJ10	Yes	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AH10	Yes	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AW4	Yes	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AV5	Yes	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AE12	Yes	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AE13	Yes	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	AT5	Yes	DQSn7R			
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	AR5	Yes	DQS7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AD12	Yes	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AD13	Yes	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AW5	Yes				
5A	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AW6	Yes				
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AH8	Yes	DQ8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AH9	Yes	DQ8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	AP5	Yes	DQSn8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	AP6	Yes	DQS8R	DQ8R/CQn8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	AK7	Yes	DQ8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	AK8	Yes	DQ8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R14n	DIFFOUT_R28n	AM5	Yes	DQSn9R	DQSn8R/DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R14p	DIFFOUT_R28p	AM6	Yes	DQS9R	DQS8R/CQ8R	DQ8R/CQn8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R15n	DIFFOUT_R29n	AE10	Yes	DQ9R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R15p	DIFFOUT_R29p	AE11	Yes	DQ9R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R15n	DIFFOUT_R30n	AN5	Yes	DQ9R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R15p	DIFFOUT_R30p	AN6	Yes	DQ9R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R31n	AF10	Yes	DQ10R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R31p	AF11	Yes	DQ10R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R32n	AL5	Yes	DQSn10R	DQ9R	DQSn8R/DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R32p	AL6	Yes	DQS10R	DQ9R/CQn9R	DQS8R/CQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R33n	AG9	Yes	DQ10R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	AG10	Yes	DQ10R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	AK5	Yes	DQSn11R	DQSn9R/DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	AK6	Yes	DQS11R	DQS9R/CQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R35n	AD9	Yes	DQ11R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	AD10	Yes	DQ11R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R36n	AJ5	Yes	DQ11R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R36p	AJ6	Yes	DQ11R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	AG7	Yes	DQ12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	AG8	Yes	DQ12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	AC8	Yes	DQSn12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	AB9	Yes	DQS12R	DQ10R/CQn10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	AB10	Yes	DQ12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	AB11	Yes	DQ12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R40n	AH5	Yes	DQSn13R	DQSn10R/DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	AH6	Yes	DQS13R	DQS10R/CQ10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	AB12	Yes	DQ13R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	AB13	Yes	DQ13R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R21n	DIFFOUT_R42n	AG5	Yes	DQ13R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	AG6	Yes	DQ13R	DQ10R		
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	AC10	No				
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	AC11	No				
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R22n	DIFFOUT_R44n	AE5	No				
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R22p	DIFFOUT_R44p	AF6	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
5C	VREFB5CN0	CLK8n	CLK8n				AC5	No				
5C	VREFB5CN0	CLK8p	CLK8p				AC6	No				
6C	VREFB6CN0	CLK10p	CLK10p				AB6	No				
6C	VREFB6CN0	CLK10n	CLK10n				AA5	No				
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	W6	No				
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	W5	No				
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	W12	No				
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	W11	No				
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	W8	Yes	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	W7	Yes	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	V12	Yes	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	V11	Yes	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	V6	Yes	DQS14R	DQS17R/CQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	U5	Yes	DQSn14R	DQSn17R/DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	U10	Yes	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	T9	Yes	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	R6	Yes	DQS15R	DQ17R/CQn17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	R5	Yes	DQSn15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	V10	Yes	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	V9	Yes	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	R7	Yes	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	P6	Yes	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	N9	Yes	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	P8	Yes	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	N6	Yes	DQS16R	DQS18R/CQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	N5	Yes	DQSn16R	DQSn18R/DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	T10	Yes	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	R10	Yes	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	M6	Yes	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R29n	DIFFOUT_R57n	L5	Yes	DQSn17R	DQ18R	DQSn19R/DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R29p	DIFFOUT_R58p	R9	Yes	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R29n	DIFFOUT_R58n	R8	Yes	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	N8	Yes	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	N7	Yes	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	M8	Yes	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	M7	Yes	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	K6	Yes	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R31n	DIFFOUT_R61n	K5	Yes	DQSn18R	DQSn19R/DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	L8	Yes	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	L7	Yes	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	J6	Yes	DQS19R	DQ19R/CQn19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	J5	Yes	DQSn19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	K7	Yes	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	J7	Yes	DQ19R	DQ19R	DQ19R	
6A	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	T13	Yes	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	T12	Yes	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	F7	Yes	DQS20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	E7	Yes	DQSn20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	H7	Yes	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	G7	Yes	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	G5	Yes	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R69n	F5	Yes	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	R13	Yes	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	P13	Yes	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	G6	Yes	DQS21R	DQS24R/CQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	F6	Yes	DQSn21R	DQSn24R/DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	R12	Yes	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	R11	Yes	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	G9	Yes	DQS22R	DQ24R/CQn24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	F9	Yes	DQSn22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	N11	Yes	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	N10	Yes	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	F10	Yes	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	E10	Yes	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	M10	Yes	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	L10	Yes	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	D7	Yes	DQS23R	DQS25R/CQ25R	DQ26R	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	C7	Yes	DQSn23R	DQSn25R/DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	K9	Yes	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	J9	Yes	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	D8	Yes	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	C8	Yes	DQSn24R	DQ25R	DQSn26R/DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	K8	Yes	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	J8	Yes	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	D9	Yes	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	C9	Yes	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	M11	Yes	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	L11	Yes	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	D5	Yes	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	C5	Yes	DQSn25R	DQSn26R/DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	N12	Yes	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	M12	Yes	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D10	Yes	DQS26R	DQ26R/CQn26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	C10	Yes	DQSn26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	K10	Yes	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	J10	Yes	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	D6	Yes				
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	C6	Yes				
6A	VREFB6AN0	IO	PLL_R1_FB_CLKOUT0p		DIFFIO_TX_R44p	DIFFOUT_R88p	H10	Yes				
6A	VREFB6AN0	IO	PLL_R1_CLKOUT0n		DIFFIO_TX_R44n	DIFFOUT_R88n	G10	Yes				
		MSEL2		MSEL2			A8	No				
		MSEL1		MSEL1			H11	No				
		MSEL0		MSEL0			J11	No				
7A	VREFB7AN0	IO				DIFFOUT_T1n	M13	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	N13	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	N14	Yes	DQSn1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	P14	Yes	DQS1T	DQ1T/CQn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	N15	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	R14	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	K13	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	L13	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	K12	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	M14	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	K14	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	L14	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	J13	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	J12	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	G13	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	H13	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	G14	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	H14	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	E13	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	F13	Yes	DQS4T	DQS2T/CQ2T	DQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	D13	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	F12	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	E14	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	F14	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	C11	Yes	DQ5T	DQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13p	A10	Yes	DQ5T	DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	A11	Yes	DQSn5T	DQ3T		DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	B11	Yes	DQS5T	DQ3T/CQn3T		DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T15n	B10	Yes	DQ5T	DQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T15p	D11	Yes	DQ5T	DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	C14	Yes	DQSn6T	DQSn3T/DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	D14	Yes	DQS6T	DQS3T/CQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T17n	C13	Yes	DQ6T	DQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T17p	C12	Yes	DQ6T	DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A13	Yes	DQ6T	DQ3T		DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B13	Yes	DQ6T	DQ3T		DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T19n	J15	Yes				DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T19p	K15	Yes				DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	A14	Yes				DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	B14	Yes				DQ1T
7B	VREFB7BN0	IO				DIFFOUT_T25n	G15	Yes	DQ9T	DQ9T	DQ9T	

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
7B	VREFB7BN0	IO				DIFFOUT_T25p	E16	Yes	DQ9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	F16	Yes	DQSn9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	G16	Yes	DQS9T	DQ9T/CQn9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T27n	G17	Yes	DQ9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T27p	F15	Yes	DQ9T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	C15	Yes	DQSn10T	DQSn9T/DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	D15	Yes	DQS10T	DQS9T/CQ9T	DQ9T/CQn9T	
7B	VREFB7BN0	IO				DIFFOUT_T29n	A16	Yes	DQ10T	DQ9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T29p	D16	Yes	DQ10T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	B16	Yes	DQ10T	DQ9T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	C16	Yes	DQ10T	DQ9T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T31n	P16	Yes	DQ11T	DQ10T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T31p	P17	Yes	DQ11T	DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	M16	Yes	DQSn11T	DQ10T	DQSn9T/DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	N16	Yes	DQS11T	DQ10T/CQn10T	DQS9T/CQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T33n	N17	Yes	DQ11T	DQ10T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T33p	M17	Yes	DQ11T	DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	J16	Yes	DQSn12T	DQSn10T/DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	K16	Yes	DQS12T	DQS10T/CQ10T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T35n	K17	Yes	DQ12T	DQ10T	DQ9T	
7B	VREFB7BN0	IO				DIFFOUT_T35p	L16	Yes	DQ12T	DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	H17	Yes	DQ12T	DQ10T	DQ9T	
7B	VREFB7BN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	J17	Yes	DQ12T	DQ10T	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T49n	C17	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T49p	F17	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	D17	Yes	DQSn17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	E17	Yes	DQS17T	DQ17T/CQn17T		
7C	VREFB7CN0	IO				DIFFOUT_T51n	C18	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T51p	D18	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	F18	Yes	DQSn18T	DQSn17T/DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	G18	Yes	DQS18T	DQS17T/CQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T53n	G20	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T53p	F20	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	F19	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	G19	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T55n	R18	Yes	DQ19T			
7C	VREFB7CN0	IO				DIFFOUT_T55p	J18	Yes	DQ19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	A17	Yes	DQSn19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	B17	Yes	DQS19T			
7C	VREFB7CN0	IO				DIFFOUT_T57n	H19	Yes	DQ19T			
7C	VREFB7CN0	IO				DIFFOUT_T57p	P18	Yes	DQ19T			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T59n	M19	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T59p	L19	No				
7C	VREFB7CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T60n	C19	No				
7C	VREFB7CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T60p	D19	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T61n	N19	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T61p	P19	No				
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T31n	DIFFOUT_T62n	C20	No				
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T31p	DIFFOUT_T62p	D20	No				
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	A19	No				
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	B20	No				
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	A20	No				
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	A21	No				
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	B22	No				
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	A22	No				
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	B23	No				
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	A23	No				
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	G21	No				
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	F21	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	M20	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	L20	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	D21	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	C22	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	N20	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	P20	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	A25	Yes				
8C	VREFB8CN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	A24	Yes				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
8C	VREFB8CN0	IO				DIFFOUT_T72p	M21	Yes	DQ20T			
8C	VREFB8CN0	IO				DIFFOUT_T72n	R20	Yes	DQ20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	D24	Yes	DQS20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	C24	Yes	DQSn20T			
8C	VREFB8CN0	IO				DIFFOUT_T74p	N21	Yes	DQ20T			
8C	VREFB8CN0	IO				DIFFOUT_T74n	M22	Yes	DQ20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	J22	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	H22	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T76p	G22	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T76n	K22	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	J23	Yes	DQS21T	DQS22T/CQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	H23	Yes	DQSn21T	DQSn22T/DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T78p	E22	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T78n	D22	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	E23	Yes	DQS22T	DQ22T/CQn22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	D23	Yes	DQSn22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T80p	G23	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T80n	F23	Yes	DQ22T	DQ22T		
8B	VREFB8BN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	K24	Yes	DQ27T	DQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	J24	Yes	DQ27T	DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T94p	M24	Yes	DQ27T	DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T94n	J25	Yes	DQ27T	DQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T95p	L23	Yes	DQS27T	DQS29T/CQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T95n	K23	Yes	DQSn27T	DQSn29T/DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T96p	N22	Yes	DQ28T	DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T96n	M23	Yes	DQ28T	DQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T49p	DIFFOUT_T97p	P23	Yes	DQS28T	DQ29T/CQn29T	DQS30T/CQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T49n	DIFFOUT_T97n	N23	Yes	DQSn28T	DQ29T	DQSn30T/DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T98p	R22	Yes	DQ28T	DQ29T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T98n	P22	Yes	DQ28T	DQ29T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T50p	DIFFOUT_T99p	G24	Yes	DQ29T	DQ30T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T50n	DIFFOUT_T99n	F24	Yes	DQ29T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T100p	G25	Yes	DQ29T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T100n	D25	Yes	DQ29T	DQ30T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T51p	DIFFOUT_T101p	F25	Yes	DQS29T	DQS30T/CQ30T	DQ30T/CQn30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T51n	DIFFOUT_T101n	E25	Yes	DQSn29T	DQSn30T/DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T102p	C25	Yes	DQ30T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T102n	B25	Yes	DQ30T	DQ30T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T52p	DIFFOUT_T103p	C26	Yes	DQS30T	DQ30T/CQn30T	DQ30T	
8B	VREFB8BN0	IO			DIFFIO_RX_T52n	DIFFOUT_T103n	B26	Yes	DQSn30T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T104p	A26	Yes	DQ30T	DQ30T	DQ30T	
8B	VREFB8BN0	IO				DIFFOUT_T104n	D26	Yes	DQ30T	DQ30T	DQ30T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	G26	Yes				DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	F26	Yes				DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T110p	P24	Yes				DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T110n	R24	Yes				DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	A28	Yes	DQ33T	DQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	A27	Yes	DQ33T	DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T112p	C27	Yes	DQ33T	DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T112n	D27	Yes	DQ33T	DQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	C28	Yes	DQS33T	DQS36T/CQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	B28	Yes	DQSn33T	DQSn36T/DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T114p	B31	Yes	DQ34T	DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T114n	A31	Yes	DQ34T	DQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	B29	Yes	DQS34T	DQ36T/CQn36T		DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	A29	Yes	DQSn34T	DQ36T		DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T116p	C29	Yes	DQ34T	DQ36T		DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T116n	C30	Yes	DQ34T	DQ36T		DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	F28	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	E28	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	D28	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118n	F27	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	E29	Yes	DQS35T	DQS37T/CQ37T	DQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	D29	Yes	DQSn35T	DQSn37T/DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	G27	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	H26	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	H28	Yes	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T	DQ38T

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	G28	Yes	DQSn36T	DQ37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	J26	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	G29	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	L26	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	K26	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	L25	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124n	K28	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	K27	Yes	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	J27	Yes	DQSn37T	DQSn38T/DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	M25	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	N25	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	P26	Yes	DQS38T	DQ38T/CQn38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	N26	Yes	DQSn38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128p	P25	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	M27	Yes	DQ38T	DQ38T	DQ38T	DQ38T
QL2		GXB_TX_L11p					B36	No				
QL2		GXB_TX_L11n					B37	No				
QL2		GXB_RX_L11p					C38	No				
QL2		GXB_RX_L11n					C39	No				
QL2		GXB_TX_L10p					D36	No				
QL2		GXB_TX_L10n					D37	No				
QL2		GXB_RX_L10p					E38	No				
QL2		GXB_RX_L10n					E39	No				
QL2		REFCLK_L5p,GXB_CMURX_L5p					G38	No				
QL2		REFCLK_L5n,GXB_CMURX_L5n					G39	No				
QL2		REFCLK_L4p,GXB_CMURX_L4p					J38	No				
QL2		REFCLK_L4n,GXB_CMURX_L4n					J39	No				
QL2		GXB_TX_L9p					K36	No				
QL2		GXB_TX_L9n					K37	No				
QL2		GXB_RX_L9p					L38	No				
QL2		GXB_RX_L9n					L39	No				
QL2		GXB_TX_L8p					M36	No				
QL2		GXB_TX_L8n					M37	No				
QL2		GXB_RX_L8p					N38	No				
QL2		GXB_RX_L8n					N39	No				
QL1		GXB_TX_L7p					P36	No				
QL1		GXB_TX_L7n					P37	No				
QL1		GXB_RX_L7p					R38	No				
QL1		GXB_RX_L7n					R39	No				
QL1		GXB_TX_L6p					T36	No				
QL1		GXB_TX_L6n					T37	No				
QL1		GXB_RX_L6p					U38	No				
QL1		GXB_RX_L6n					U39	No				
QL1		REFCLK_L3p,GXB_CMURX_L3p					W38	No				
QL1		REFCLK_L3n,GXB_CMURX_L3n					W39	No				
QL1		REFCLK_L2p,GXB_CMURX_L2p					AA38	No				
QL1		REFCLK_L2n,GXB_CMURX_L2n					AA39	No				
QL1		GXB_TX_L5p					AB36	No				
QL1		GXB_TX_L5n					AB37	No				
QL1		GXB_RX_L5p					AC38	No				
QL1		GXB_RX_L5n					AC39	No				
QL1		GXB_TX_L4p					AD36	No				
QL1		GXB_TX_L4n					AD37	No				
QL1		GXB_RX_L4p					AE38	No				
QL1		GXB_RX_L4n					AE39	No				
QL0		GXB_TX_L3p					AF36	No				
QL0		GXB_TX_L3n					AF37	No				
QL0		GXB_RX_L3p					AG38	No				
QL0		GXB_RX_L3n					AG39	No				
QL0		GXB_TX_L2p					AH36	No				
QL0		GXB_TX_L2n					AH37	No				
QL0		GXB_RX_L2p					AJ38	No				
QL0		GXB_RX_L2n					AJ39	No				
QL0		REFCLK_L1p,GXB_CMURX_L1p					AL38	No				
QL0		REFCLK_L1n,GXB_CMURX_L1n					AL39	No				
QL0		REFCLK_L0p,GXB_CMURX_L0p					AN38	No				
QL0		REFCLK_L0n,GXB_CMURX_L0n					AN39	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
QL0		GXB_TX_L1p					AP36	No				
QL0		GXB_TX_L1n					AP37	No				
QL0		GXB_RX_L1p					AR38	No				
QL0		GXB_RX_L1n					AR39	No				
QL0		GXB_TX_L0p					AT36	No				
QL0		GXB_TX_L0n					AT37	No				
QL0		GXB_RX_L0p					AU38	No				
QL0		GXB_RX_L0n					AU39	No				
QR0		GXB_RX_R0n					AU1	No				
QR0		GXB_RX_R0p					AU2	No				
QR0		GXB_TX_R0n					AT3	No				
QR0		GXB_TX_R0p					AT4	No				
QR0		GXB_RX_R1n					AR1	No				
QR0		GXB_RX_R1p					AR2	No				
QR0		GXB_TX_R1n					AP3	No				
QR0		GXB_TX_R1p					AP4	No				
QR0		REFCLK_R0n,GXB_CMURX_R0n					AN1	No				
QR0		REFCLK_R0p,GXB_CMURX_R0p					AN2	No				
QR0		REFCLK_R1n,GXB_CMURX_R1n					AL1	No				
QR0		REFCLK_R1p,GXB_CMURX_R1p					AL2	No				
QR0		GXB_RX_R2n					AJ1	No				
QR0		GXB_RX_R2p					AJ2	No				
QR0		GXB_TX_R2n					AH3	No				
QR0		GXB_TX_R2p					AH4	No				
QR0		GXB_RX_R3n					AG1	No				
QR0		GXB_RX_R3p					AG2	No				
QR0		GXB_TX_R3n					AF3	No				
QR0		GXB_TX_R3p					AF4	No				
QR1		GXB_RX_R4n					AE1	No				
QR1		GXB_RX_R4p					AE2	No				
QR1		GXB_TX_R4n					AD3	No				
QR1		GXB_TX_R4p					AD4	No				
QR1		GXB_RX_R5n					AC1	No				
QR1		GXB_RX_R5p					AC2	No				
QR1		GXB_TX_R5n					AB3	No				
QR1		GXB_TX_R5p					AB4	No				
QR1		REFCLK_R2n,GXB_CMURX_R2n					AA1	No				
QR1		REFCLK_R2p,GXB_CMURX_R2p					AA2	No				
QR1		REFCLK_R3n,GXB_CMURX_R3n					W1	No				
QR1		REFCLK_R3p,GXB_CMURX_R3p					W2	No				
QR1		GXB_RX_R6n					U1	No				
QR1		GXB_RX_R6p					U2	No				
QR1		GXB_TX_R6n					T3	No				
QR1		GXB_TX_R6p					T4	No				
QR1		GXB_RX_R7n					R1	No				
QR1		GXB_RX_R7p					R2	No				
QR1		GXB_TX_R7n					P3	No				
QR1		GXB_TX_R7p					P4	No				
QR2		GXB_RX_R8n					N1	No				
QR2		GXB_RX_R8p					N2	No				
QR2		GXB_TX_R8n					M3	No				
QR2		GXB_TX_R8p					M4	No				
QR2		GXB_RX_R9n					L1	No				
QR2		GXB_RX_R9p					L2	No				
QR2		GXB_TX_R9n					K3	No				
QR2		GXB_TX_R9p					K4	No				
QR2		REFCLK_R4n,GXB_CMURX_R4n					J1	No				
QR2		REFCLK_R4p,GXB_CMURX_R4p					J2	No				
QR2		REFCLK_R5n,GXB_CMURX_R5n					G1	No				
QR2		REFCLK_R5p,GXB_CMURX_R5p					G2	No				
QR2		GXB_RX_R10n					E1	No				
QR2		GXB_RX_R10p					E2	No				
QR2		GXB_TX_R10n					D3	No				
QR2		GXB_TX_R10p					D4	No				
QR2		GXB_RX_R11n					C1	No				
QR2		GXB_RX_R11p					C2	No				
QR2		GXB_TX_R11n					B3	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
QR2		GXB_TX_R11p					B4	No				
		GND					AL11	No				
		GND					Y21	No				
		GND					AV6	No				
		GND					AV9	No				
		GND					AV12	No				
		GND					AV15	No				
		GND					AV18	No				
		GND					AV21	No				
		GND					AV24	No				
		GND					AV27	No				
		GND					AV30	No				
		GND					AV33	No				
		GND					AR6	No				
		GND					AR9	No				
		GND					AR12	No				
		GND					AR15	No				
		GND					AR18	No				
		GND					AR21	No				
		GND					AR24	No				
		GND					AR27	No				
		GND					AR30	No				
		GND					AR33	No				
		GND					AM7	No				
		GND					AM9	No				
		GND					AM12	No				
		GND					AM15	No				
		GND					AM18	No				
		GND					AM21	No				
		GND					AM24	No				
		GND					AM27	No				
		GND					AM30	No				
		GND					AM33	No				
		GND					AJ7	No				
		GND					AJ9	No				
		GND					AJ12	No				
		GND					AJ15	No				
		GND					AJ18	No				
		GND					AJ21	No				
		GND					AJ24	No				
		GND					AJ27	No				
		GND					AJ30	No				
		GND					AJ33	No				
		GND					AF9	No				
		GND					AF12	No				
		GND					AF15	No				
		GND					AF18	No				
		GND					AF21	No				
		GND					AF24	No				
		GND					AF27	No				
		GND					AF30	No				
		GND					AD23	No				
		GND					AC7	No				
		GND					AC9	No				
		GND					AC12	No				
		GND					AC14	No				
		GND					AC16	No				
		GND					AC18	No				
		GND					AC20	No				
		GND					AC22	No				
		GND					AC24	No				
		GND					AC27	No				
		GND					AC30	No				
		GND					AC33	No				
		GND					AB15	No				
		GND					AB17	No				
		GND					AB19	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		GND					AB21	No				
		GND					AB23	No				
		GND					AB25	No				
		GND					AA14	No				
		GND					AA16	No				
		GND					AA18	No				
		GND					AA22	No				
		GND					AA24	No				
		GND					Y12	No				
		GND					Y15	No				
		GND					Y17	No				
		GND					Y19	No				
		GND					Y23	No				
		GND					Y25	No				
		GND					Y27	No				
		GND					Y30	No				
		GND					W10	No				
		GND					W14	No				
		GND					W16	No				
		GND					W18	No				
		GND					W20	No				
		GND					W22	No				
		GND					W24	No				
		GND					V15	No				
		GND					V17	No				
		GND					V19	No				
		GND					V21	No				
		GND					V23	No				
		GND					V25	No				
		GND					U9	No				
		GND					U12	No				
		GND					U14	No				
		GND					U16	No				
		GND					U18	No				
		GND					U20	No				
		GND					U22	No				
		GND					U24	No				
		GND					U26	No				
		GND					U28	No				
		GND					U30	No				
		GND					T15	No				
		GND					T17	No				
		GND					T19	No				
		GND					T21	No				
		GND					T23	No				
		GND					T25	No				
		GND					P7	No				
		GND					P9	No				
		GND					P12	No				
		GND					P15	No				
		GND					P21	No				
		GND					P27	No				
		GND					P30	No				
		GND					P33	No				
		GND					N18	No				
		GND					N24	No				
		GND					L6	No				
		GND					L9	No				
		GND					L12	No				
		GND					L15	No				
		GND					L18	No				
		GND					L21	No				
		GND					L24	No				
		GND					L27	No				
		GND					L30	No				
		GND					L33	No				
		GND					H6	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		GND					H9	No				
		GND					H12	No				
		GND					H15	No				
		GND					H18	No				
		GND					H21	No				
		GND					H24	No				
		GND					H27	No				
		GND					H30	No				
		GND					H33	No				
		GND					E6	No				
		GND					E9	No				
		GND					E12	No				
		GND					E15	No				
		GND					E18	No				
		GND					E21	No				
		GND					E24	No				
		GND					E27	No				
		GND					E30	No				
		GND					E33	No				
		GND					B9	No				
		GND					B12	No				
		GND					B15	No				
		GND					B18	No				
		GND					B21	No				
		GND					B24	No				
		GND					B27	No				
		GND					B30	No				
		GND					H35	No				
		GND					H34	No				
		GND					AW23	No				
		GND					AV23	No				
		GND					AT19	No				
		GND					AU19	No				
		GND					G8	No				
		GND					F8	No				
		GND					A18	No				
		GND					B19	No				
		GND					E11	No				
		GND					A9	No				
		GND					A38	No				
		GND					A37	No				
		GND					A36	No				
		GND					A35	No				
		GND					A33	No				
		GND					B39	No				
		GND					B38	No				
		GND					B35	No				
		GND					B34	No				
		GND					B33	No				
		GND					C37	No				
		GND					C36	No				
		GND					D39	No				
		GND					D38	No				
		GND					E37	No				
		GND					E36	No				
		GND					F39	No				
		GND					AW37	No				
		GND					AV37	No				
		GND					AV38	No				
		GND					AV39	No				
		GND					AU36	No				
		GND					AU37	No				
		GND					AT38	No				
		GND					AT39	No				
		GND					AR36	No				
		GND					AR37	No				
		GND					AP38	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		GND					AP39	No				
		GND					AN36	No				
		GND					AN37	No				
		GND					AM38	No				
		GND					AM39	No				
		GND					AL36	No				
		GND					AL37	No				
		GND					AK38	No				
		GND					AK39	No				
		GND					AJ36	No				
		GND					AJ37	No				
		GND					AH38	No				
		GND					AH39	No				
		GND					AG36	No				
		GND					AG37	No				
		GND					AF33	No				
		GND					AF38	No				
		GND					AF39	No				
		GND					AE36	No				
		GND					AE37	No				
		GND					AD32	No				
		GND					AD34	No				
		GND					AD38	No				
		GND					AD39	No				
		GND					AC36	No				
		GND					AC37	No				
		GND					AB33	No				
		GND					AB38	No				
		GND					AB39	No				
		GND					AA36	No				
		GND					AA37	No				
		GND					Y32	No				
		GND					Y34	No				
		GND					Y38	No				
		GND					Y39	No				
		GND					W36	No				
		GND					W37	No				
		GND					V33	No				
		GND					V38	No				
		GND					V39	No				
		GND					U36	No				
		GND					U37	No				
		GND					T32	No				
		GND					T34	No				
		GND					T38	No				
		GND					T39	No				
		GND					R36	No				
		GND					R37	No				
		GND					P38	No				
		GND					P39	No				
		GND					N36	No				
		GND					N37	No				
		GND					M38	No				
		GND					M39	No				
		GND					L36	No				
		GND					L37	No				
		GND					K38	No				
		GND					K39	No				
		GND					J36	No				
		GND					J37	No				
		GND					H38	No				
		GND					H39	No				
		GND					G36	No				
		GND					G37	No				
		GND					F38	No				
		GND					A7	No				
		GND					A5	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		GND					A4	No				
		GND					A3	No				
		GND					A2	No				
		GND					B7	No				
		GND					B6	No				
		GND					B5	No				
		GND					B2	No				
		GND					B1	No				
		GND					C4	No				
		GND					C3	No				
		GND					D2	No				
		GND					D1	No				
		GND					E4	No				
		GND					E3	No				
		GND					F2	No				
		GND					AW3	No				
		GND					AV1	No				
		GND					AV2	No				
		GND					AV3	No				
		GND					AU3	No				
		GND					AU4	No				
		GND					AT1	No				
		GND					AT2	No				
		GND					AR3	No				
		GND					AR4	No				
		GND					AP1	No				
		GND					AP2	No				
		GND					AN3	No				
		GND					AN4	No				
		GND					AM1	No				
		GND					AM2	No				
		GND					AL3	No				
		GND					AL4	No				
		GND					AK1	No				
		GND					AK2	No				
		GND					AJ3	No				
		GND					AJ4	No				
		GND					AH1	No				
		GND					AH2	No				
		GND					AG3	No				
		GND					AG4	No				
		GND					AF1	No				
		GND					AF2	No				
		GND					AF7	No				
		GND					AE3	No				
		GND					AE4	No				
		GND					AD1	No				
		GND					AD2	No				
		GND					AD6	No				
		GND					AD8	No				
		GND					AC3	No				
		GND					AC4	No				
		GND					AB1	No				
		GND					AB2	No				
		GND					AB7	No				
		GND					AA3	No				
		GND					AA4	No				
		GND					Y1	No				
		GND					Y2	No				
		GND					Y6	No				
		GND					Y8	No				
		GND					W3	No				
		GND					W4	No				
		GND					V1	No				
		GND					V2	No				
		GND					V7	No				
		GND					U3	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		GND					U4	No				
		GND					T1	No				
		GND					T2	No				
		GND					T6	No				
		GND					T8	No				
		GND					R3	No				
		GND					R4	No				
		GND					P1	No				
		GND					P2	No				
		GND					N3	No				
		GND					N4	No				
		GND					M1	No				
		GND					M2	No				
		GND					L3	No				
		GND					L4	No				
		GND					K1	No				
		GND					K2	No				
		GND					J3	No				
		GND					J4	No				
		GND					H1	No				
		GND					H2	No				
		GND					G3	No				
		GND					G4	No				
		GND					F1	No				
		GND					W9	No				
		GND					Y9	No				
		GND					AA9	No				
		VCC					Y20	No				
		VCC					AC15	No				
		VCC					AC17	No				
		VCC					AC25	No				
		VCC					AB14	No				
		VCC					AB16	No				
		VCC					AB18	No				
		VCC					AB20	No				
		VCC					AB22	No				
		VCC					AB24	No				
		VCC					AA15	No				
		VCC					AA19	No				
		VCC					AA21	No				
		VCC					AA25	No				
		VCC					Y14	No				
		VCC					Y16	No				
		VCC					Y18	No				
		VCC					Y22	No				
		VCC					Y24	No				
		VCC					W15	No				
		VCC					W19	No				
		VCC					W21	No				
		VCC					W25	No				
		VCC					V14	No				
		VCC					V16	No				
		VCC					V18	No				
		VCC					V20	No				
		VCC					V22	No				
		VCC					V24	No				
		VCC					V26	No				
		VCC					U15	No				
		VCC					U19	No				
		VCC					U21	No				
		VCC					U25	No				
		VCC					T14	No				
		VCC					T16	No				
		VCC					T24	No				
		VCC					T26	No				
		VCC					T18	No				
		VCC					AC19	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		VCC					AC21	No				
		VCC					AC23	No				
		VCC					AA17	No				
		VCC					AA23	No				
		VCC					W17	No				
		VCC					W23	No				
		VCC					U17	No				
		VCC					U23	No				
		VCC					T20	No				
		VCC					T22	No				
		VCC					AA32	No				
		VCC					AF32	No				
		VCC					AE32	No				
		VCC					AB32	No				
		VCC					V32	No				
		VCC					U32	No				
		VCC					AF8	No				
		VCC					AE8	No				
		VCC					AB8	No				
		VCC					AA8	No				
		VCC					V8	No				
		VCC					U8	No				
		DNU					AA20	No				
		VCCPGM					AK28	No				
		VCCPGM					AK12	No				
		VCC_CLKIN3C					AK21	No				
		VCC_CLKIN4C					AK18	No				
		VCC_CLKIN7C					K18	No				
		VCC_CLKIN8C					K21	No				
		VCCBAT					K11	No				
		VCCA_PLL_B1					AL20	No				
		VCCA_PLL_B2					AL19	No				
		VCCA_PLL_L2					Y29	No				
		VCCA_PLL_L3					AA29	No				
		VCCA_PLL_R2					Y10	No				
		VCCA_PLL_R3					AA10	No				
		VCCA_PLL_T1					J20	No				
		VCCA_PLL_T2					J19	No				
		VCCD_PLL_B1					AK20	No				
		VCCD_PLL_B2					AK19	No				
		VCCD_PLL_L2					Y28	No				
		VCCD_PLL_L3					AA28	No				
		VCCD_PLL_R2					Y11	No				
		VCCD_PLL_R3					AA11	No				
		VCCD_PLL_T1					K20	No				
		VCCD_PLL_T2					K19	No				
		VCCIO1A					J31	No				
		VCCIO1A					G32	No				
		VCCIO1A					G34	No				
		VCCIO1A					E35	No				
		VCCIO1A					D32	No				
		VCCIO1C					AA30	No				
		VCCIO1C					T29	No				
		VCCIO1C					N32	No				
		VCCIO1C					K33	No				
		VCCIO2A					AT35	No				
		VCCIO2A					AP31	No				
		VCCIO2A					AM32	No				
		VCCIO2A					AJ28	No				
		VCCIO2A					AG26	No				
		VCCIO2C					AL33	No				
		VCCIO2C					AH31	No				
		VCCIO2C					AG33	No				
		VCCIO2C					AF31	No				
		VCCIO3A					AU30	No				
		VCCIO3A					AR29	No				
		VCCIO3A					AL26	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		VCCIO3A					AH25	No				
		VCCIO3B					AR26	No				
		VCCIO3B					AG23	No				
		VCCIO3C					AW24	No				
		VCCIO3C					AK22	No				
		VCCIO3C					AH21	No				
		VCCIO4A					AU13	No				
		VCCIO4A					AP12	No				
		VCCIO4A					AK15	No				
		VCCIO4A					AH15	No				
		VCCIO4B					AW15	No				
		VCCIO4B					AJ17	No				
		VCCIO4C					AW17	No				
		VCCIO4C					AU21	No				
		VCCIO4C					AJ19	No				
		VCCIO5A					AW9	No				
		VCCIO5A					AR7	No				
		VCCIO5A					AR10	No				
		VCCIO5A					AN8	No				
		VCCIO5A					AK10	No				
		VCCIO5C					AL7	No				
		VCCIO5C					AJ8	No				
		VCCIO5C					AH7	No				
		VCCIO5C					AE9	No				
		VCCIO6A					M9	No				
		VCCIO6A					H8	No				
		VCCIO6A					E5	No				
		VCCIO6A					E8	No				
		VCCIO6A					B8	No				
		VCCIO6C					V13	No				
		VCCIO6C					T11	No				
		VCCIO6C					P10	No				
		VCCIO6C					H5	No				
		VCCIO7A					M15	No				
		VCCIO7A					J14	No				
		VCCIO7A					D12	No				
		VCCIO7A					A12	No				
		VCCIO7B					L17	No				
		VCCIO7B					A15	No				
		VCCIO7C					M18	No				
		VCCIO7C					E19	No				
		VCCIO7C					C21	No				
		VCCIO8A					M26	No				
		VCCIO8A					J28	No				
		VCCIO8A					D30	No				
		VCCIO8A					A30	No				
		VCCIO8B					K25	No				
		VCCIO8B					E26	No				
		VCCIO8C					L22	No				
		VCCIO8C					F22	No				
		VCCIO8C					C23	No				
		VCCPD1A					U27	No				
		VCCPD1C					W27	No				
		VCCPD2A					AB26	No				
		VCCPD2C					Y26	No				
		VCCPD3A					AD24	No				
		VCCPD3B					AD22	No				
		VCCPD3C					AD20	No				
		VCCPD4A					AD14	No				
		VCCPD4B					AD16	No				
		VCCPD4C					AD18	No				
		VCCPD5A					AC13	No				
		VCCPD5C					AA13	No				
		VCCPD6A					U13	No				
		VCCPD6C					W13	No				
		VCCPD7A					R15	No				
		VCCPD7B					R17	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		VCCPD7C					R19	No				
		VCCPD8A					R25	No				
		VCCPD8B					R23	No				
		VCCPD8C					R21	No				
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				P28	No				
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				U29	No				
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AF28	No				
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				AB29	No				
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AN28	No				
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AL24	No				
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AP22	No				
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AN12	No				
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AM16	No				
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AL18	No				
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AG11	No				
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AD11	No				
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				P11	No				
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				U11	No				
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G12	No				
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				H16	No				
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				E20	No				
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				F29	No				
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				H25	No				
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				J21	No				
		NC					L28	No				
		NC					AM28	No				
		NC					AK11	No				
		NC					F11	No				
		NC					F36	No				
		NC					F37	No				
		NC					H36	No				
		NC					H37	No				
		NC					V36	No				
		NC					V37	No				
		NC					Y36	No				
		NC					Y37	No				
		NC					AK36	No				
		NC					AK37	No				
		NC					AM36	No				
		NC					AM37	No				
		NC					AV36	No				
		NC					AU35	No				
		NC					AU5	No				
		NC					AV4	No				
		NC					AM3	No				
		NC					AM4	No				
		NC					AK3	No				
		NC					AK4	No				
		NC					Y3	No				
		NC					Y4	No				
		NC					V3	No				
		NC					V4	No				
		NC					H3	No				
		NC					H4	No				
		NC					F3	No				
		NC					F4	No				
		NC					AD17	No				
		NC					R16	No				
		NC					R26	No				
		VCCAUX					H29	No				
		VCCAUX					AL28	No				
		VCCAUX					AL12	No				
		VCCAUX					G11	No				
		VCCA_L					M35	No				
		VCCA_L					AF35	No				
		VCCA_R					M5	No				
		VCCA_R					AF5	No				

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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517	DQS for X32/ X36 for F1517 *(3)*
		VCCH_GXBL0					AE34	No				
		VCCH_GXBL1					AA34	No				
		VCCH_GXBL2					U34	No				
		VCCH_GXBR0					AE6	No				
		VCCH_GXBR1					AA6	No				
		VCCH_GXBR2					U6	No				
		VCCL_GXBL0					AD33	No				
		VCCL_GXBL0					AE33	No				
		VCCL_GXBL1					Y33	No				
		VCCL_GXBL1					AA33	No				
		VCCL_GXBL2					T33	No				
		VCCL_GXBL2					U33	No				
		VCCL_GXBR0					AD7	No				
		VCCL_GXBR0					AE7	No				
		VCCL_GXBR1					Y7	No				
		VCCL_GXBR1					AA7	No				
		VCCL_GXBR2					T7	No				
		VCCL_GXBR2					U7	No				
		VCCR_L					T35	No				
		VCCR_L					Y35	No				
		VCCR_L					AD35	No				
		VCCR_R					T5	No				
		VCCR_R					Y5	No				
		VCCR_R					AD5	No				
		VCCT_L					P35	No				
		VCCT_L					V35	No				
		VCCT_L					AB35	No				
		VCCT_R					P5	No				
		VCCT_R					V5	No				
		VCCT_R					AB5	No				
		VCCHIP_L					W31	No				
		VCCHIP_L					Y31	No				
		VCCHIP_L					AA31	No				
		RREF_L0					AW38	No				
		RREF_L1					A34	No				
		RREF_R0					AW2	No				
		RREF_R1					A6	No				
		VCCCB					AA27	No				
		VCCCB					AA26	No				
		VCCCB					AM20	No				
		VCCCB					AA12	No				
		VCCCB					Y13	No				
		VCCCB					H20	No				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the
Arria II Device Family Pin Connection Guidelines.
(2) PLL_R1/R4 and PLL_L1/L4 outputs are not available in the EP2AGZ350 device.
(3) Altera's external memory interface IPs do not support placement of the BWSn pins outside the DQS/DQ group adjacent to the x32/x36 DQS/DQ groups where the write data pins reside. When using x32/x36 DQS/DQ groups that have 40 pins, BWSn inputs are not supported. However, if you are not using Altera's memory interface IPs and you are using x32/x36 DQS/DQ groups that have 40 pins, you can place the BWSn pins in a separate ×4 DQS/DQ group adjacent to the x32/x36 DQS/DQ group where the write data pins reside.

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Version Number	Date	Changes Made
1.0	12/3/2010	Initial release.
1.1	6/18/2014	Added a note to Pin List F780, Pin List F1152, and Pin List F1517 to include detail that PLL_R1/R4 and PLL_L1/L4 outputs are not available in the EP2AGZ350 device.
1.2	2/4/2015	Added the Dynamic OCT Support column in Pin List F780, Pin List F1152, and Pin List F1517.

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