White Paper

Gain Flexibility and Increased Integration With Advanced Cyclone III FPGA PLLs

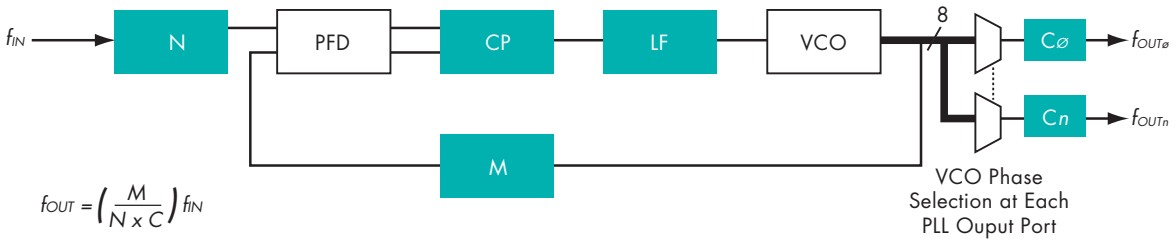
Introduction

An often-overlooked benefit of using FPGAs is the ability to integrate a clocking solution. Not only does this integration allow the reduction of the system cost, but because the latest 65-nm Altera® Cyclone® III FPGA contains advanced clock management and phase-locked loop (PLL) technology, it also allows for an amazing amount of flexibility in the design. The Cyclone III clock management system allows designers to manage the clocking system for the entire FPGA as well as on the board. Furthermore, because the Cyclone III PLLs are integrated in the FPGA, they take advantage of Altera's Quartus® II design environment, which allows easy set up and configuration.

Cyclone III PLL Clock Synthesizer Architecture

The block diagram in Figure 1 shows the Cyclone III PLL. The PLL is a feedback loop of which the main components are the phase frequency detector (PFD), the charge pump (CP), the loop filter (LF), voltage-controlled oscillator (VCO), and the feedback counter, M. The PFD looks at the phase difference between the input clock and the feedback clock and signals the PLL when they are out of alignment. The CP and LF take the signal from the PFD and create a control voltage for the VCO to create the desired output frequency and phase. The PLL contains three types of counters: the pre-scale N counter, the post-scale C counters, and the feedback M counter.

Figure 1. Cyclone III PLL Block Diagram



The highlighted blocks in the diagram indicate the user-programmable portions of the Cyclone III PLL and give the user a significant amount of design flexibility. All counters in the PLL are user programmable, allowing the synthesis of virtually any ratio of input to output clock frequency. It also allows for a wide range of acceptable input frequencies as well as the ability to generate a wide range of output frequencies. The programmable output C counters allow different frequency and/or phase clock outputs to be generated from a single clock input. The programmable loop components of the PLL allow control of the bandwidth of the PLL in order to filter or tolerate different ranges of input jitter frequencies. Many of these user-programmable components are set automatically through software, and the whole PLL can be configured easily using the Quartus II design environment.

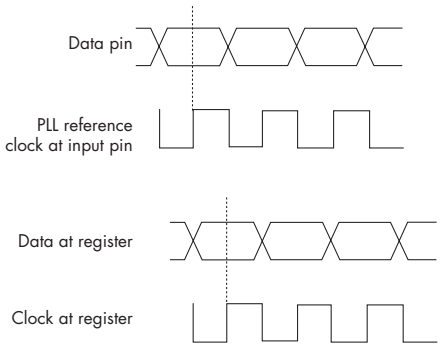
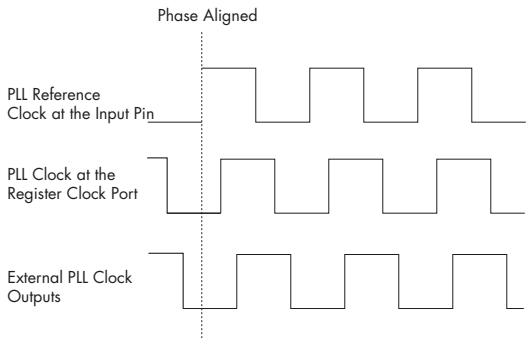
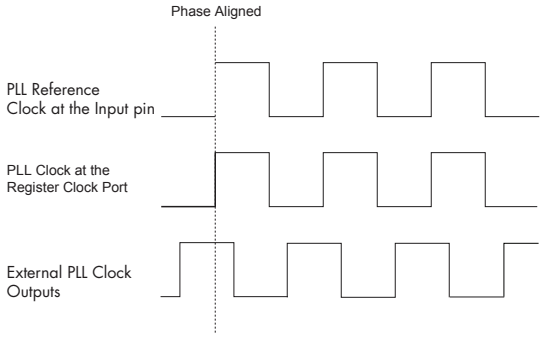
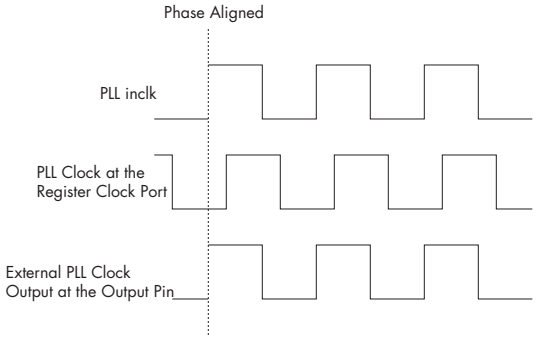
Advantages of Using Cyclone III PLLs—Flexibility, Integration, Ease of Use

A single Cyclone III PLL is a full-fledged clock synthesizer that can generate up to five clock outputs. These can feed virtually any pin on the device, allowing great flexibility in providing clocks to other devices on the board. The clock compensation modes allow the designer to adjust the phase relationship of different output clocks to the input clock of the PLL. Using the different clock compensation modes (see Table 1) offered by the PLLs, along with dedicated clock output pins, allows the designer to customize the board-clocking scheme to the application. In all but the smallest devices, Cyclone III FPGAs offer four independent PLLs per device. In addition, multiple PLLs can be cascaded to allow even more flexibility for the system's clocking needs, such as more granular clock frequencies.

Cyclone III devices also offer the flexibility of taking in a variety of different I/O standards and translating them to any other I/O standard. This allows a single clock input to interface with other chips on the board, ranging from a DDR2 SDRAM using SSTL to an LED driver using LVTTL. This eliminates the need for external components such

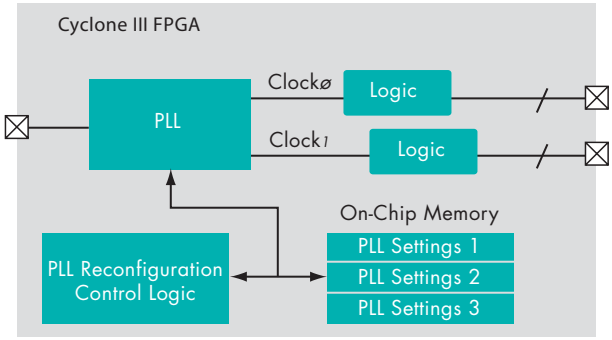
as clock drivers, voltage translators, or discrete PLLs, thereby reducing the bill of materials (and its cost), as well as the required board space.

Table 1. Clock Compensation Modes

Compensation Mode	Waveform	Description
Source Synchronous Mode		Use this mode for source-synchronous data transfers. In this mode, the phase relrelationship between data and clock at the device pins is maintained.
No Compensation Mode		Use this mode for best jitter performance. In this mode, the PLL does not compensate for any clock networks.
Normal Mode		Use this mode to align the clock at the device pins to the clock at the internal registers of the device.
Zero Delay Buffer Mode		Use this mode for zero delay through the device.

Another aspect that gives users flexibility is the Cyclone III PLL reconfiguration feature, which allows dynamic changes to the behavior of the PLL while the device is operating. Multiple PLL behavior profiles can be stored in the on-chip memory and dynamically loaded based on a system-created trigger condition. Figure 2 shows an example of this system, which operates in three different frequency modes depending on a set of fixed inputs or a user-created trigger. All three modes are supported with a single Cyclone III PLL, and each mode corresponds to a PLL profile that can be dynamically loaded in real-time. This enables a designer to create a single design for many different applications, saving valuable engineering resources and getting to market faster.

Figure 2. PLL Reconfiguration Scenario

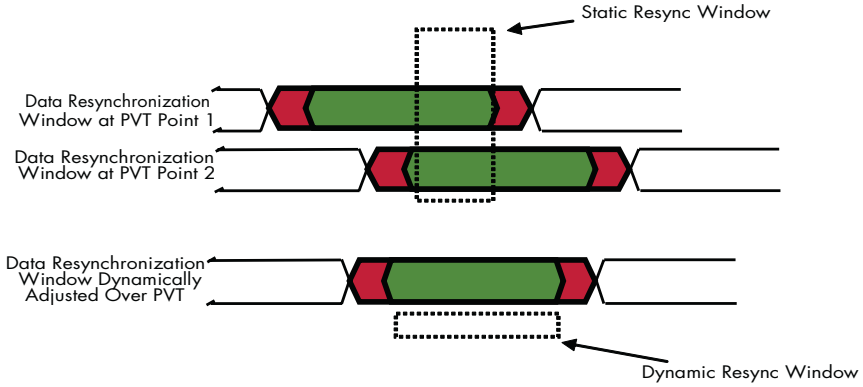


The PLL reconfiguration feature can dynamically adjust the PLL parameters to lock to a very wide spectrum of input clock frequencies. This is particularly useful in display applications where clock rates vary based on the system and the refresh rate chosen. In this case, Altera-provided IP is used to control the reconfiguration and automatically adjust the PLL parameters to lock onto the given input frequency.

Dynamic phase shifting allows adjustment of the phase of the PLL output clock on the fly, as well as tuning of the system timing after boards come back from the fab. In addition, it can be used to determine the center of the data window dynamically when transferring data to external interfaces such as DDR2 SDRAM.

Interfacing to fast DDR memories is time consuming, as the high speed and wide interface of the memories make sampling at the right time difficult. The interface also must be able to operate over process, voltage, and temperature (PVT), but it is difficult to find the exact spot to sample the data so that the memory operates correctly. Altera offers an auto-calibrating PHY that can adjust the PLL output clock phase across PVT and makes this process easier. This IP uses the dynamic phase shifting feature of the Cyclone III PLL to adjust the clock phase to calibrate the interface. This gives the best timing margin in a design and allows the interface to run at higher data rates than it otherwise could, as illustrated in Figure 3. In a non-auto-calibrating system, the data valid window is effectively smaller because the data window shifts, but the sampling point does not. The auto-calibrating system compensates for the shift, so the sampling window is effectively larger.

Figure 3. Using Dynamic Phase Shifting to Gain Timing Margin in a DDR SDRAM Interface



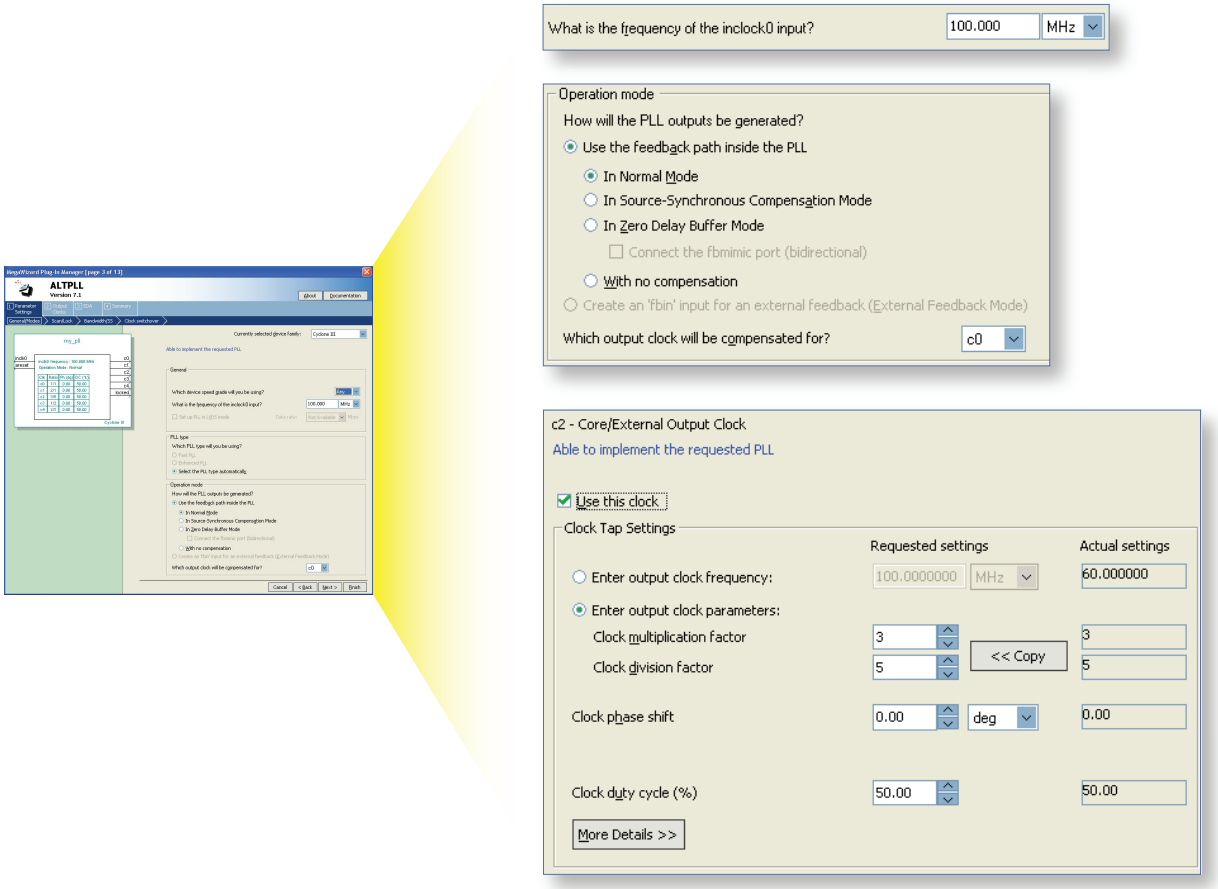
The flexibility and ease of use offered by the Cyclone III FPGA PLLs do not come at the expense of the robustness of PLL performance. Table 2 shows key Cyclone III PLL performance parameters, which allow the reduction of a system-clocking scheme to a single crystal oscillator. This PLL can generate all the clocks required for on-chip functions, as well as clocks for other chips on the board, eliminating the need for multiple crystal oscillators, other clock drivers, or discrete PLLs that have limited functionality.

Table 2. Key Cyclone III PLL Performance Parameters

Parameter	Minimum	Typical	Maximum
PLL Input Frequency Range	5 MHz		472.5 MHz
PLL Output Frequency Range	5 MHz		472.5 MHz
PLL Output Period Jitter		100 ps	
Clock Phase Shift Steps	96 ps		

Taking advantage of Cyclone III PLLs is easy through Altera's Quartus II design software. Using the software's intuitive MegaWizard® Plug-In to configure the PLL, the designer simply enters the required input and output frequency and phase relationship and the software automatically generates a PLL to suit the needs of the design. Figure 4 shows screenshots of the PLL MegaWizard configuration process. All features of a PLL can be controlled through this interface, including the setting of the desired input clock frequency, the compensation mode, the multiplication and division factors, and phase shift and duty cycle for each output clock. After customizing the PLL to suit the design needs, the designer simply clicks "Finish", instantiates the PLL in the design, compiles, and programs the device.

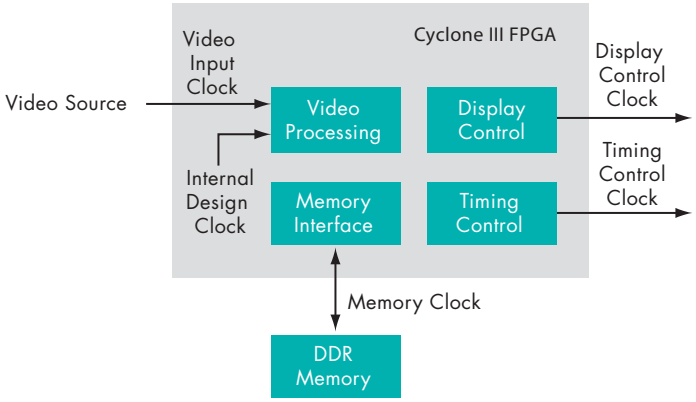
Figure 4. PLL MegaWizard Plug-In



LCD Design Example

Figure 5 shows an example of a typical application that benefits from the improved Cyclone III PLLs. The system drives a LCD display and integrates functions, such as timing controller, video processing, and a memory controller into a single Cyclone III FPGA.

Figure 5. LCD Display Design Example



This example takes advantage of several features of the Cyclone III PLL. The first is the ability to drive multiple clocks. This application has multiple clock domains that the FPGA must generate. It must be able to take in the clock frequency from the video source and generate clocks for the memory interface, the internal logic for the FPGA, and any multiple clocks the LCD display may require. Depending on the size and resolution of the LCD, the panel may have multiple clocks that need to be driven. Using the numerous outputs and multiple PLLs will allow you to generate all the clocks needed internally and externally.

The second feature is reconfigurability. In many cases, the clock rates are unknown. The video source may come in different formats with different clock frequencies, or the refresh rate and resolution of the LCD may differ from one panel to another or change on the fly. The wide frequency range of the PLL allows it to accommodate a number of different sources, as well as switch and readjust frequencies on the fly. In other FPGA architectures, the whole FPGA would need to be reconfigured to produce the right clocks, but this reconfiguration takes time and requires special design consideration. The reconfigurability of the Cyclone III PLL insures that this takes place smoothly and with minimum downtime.

This design also takes advantage of the dynamic phase-shifting capability. Video processing can be very data intensive, and the user may need to store a large amount of data off-chip. Using a second PLL in the device and Altera's auto-calibrating PHY IP to enable the FPGA adjust for PVT and sample in the optimal data window can make interfacing to DDR and DDR2 memories easy.

The logic density offered by Cyclone III devices, in conjunction with the advancements in PLL technology and the number of PLLs offered, allows this whole system to be integrated into a Cyclone III FPGA, thereby reducing costs significantly.

Summary

Like other features on Cyclone III, the PLL capabilities have advanced considerably, allowing designers to do more with a single FPGA than ever before. The combination of the PLL and FPGA fabric allows for more integration, thereby reducing costs. The ability to customize multiple outputs of the PLL gives designers a larger degree of freedom and more options on how to design. Furthermore, because Altera puts so much emphasis on software design for its FPGAs, configuring the PLLs in the system is seamless and easy.

Further Information

- Design for a Cyclone III device using the free Quartus II Web Edition software: **www.altera.com/support/software/download/sof-download_center.html**

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