11. Power Management in HardCopy III Devices

HIII51011-3.2

Altera® HardCopy® III devices and Stratix® III devices are manufactured with different process technologies. The HardCopy III devices are based on a 0.9-V, 40 nm process, while Stratix III devices are manufactured with a 1.1-V, 65 nm process. Because of the unique voltage requirements of each device family, you must design your board's power supply to support both Stratix III and HardCopy III devices. In addition, you must take into consideration that both device families consume power differently. This chapter describes the power supply requirements and power management solutions for HardCopy III devices.

This chapter contains the following sections:

- "HardCopy III Device External Power Supply Requirements"
- "Supporting HardCopy III and Stratix III Power Supplies" on page 11–2
- "HardCopy III Power Optimization" on page 11–3
- "Temperature Sensing Diode (TSD)" on page 11–4
- "External Pin Connections" on page 11–4

HardCopy III Device External Power Supply Requirements

This section describes the different external power supplies you need to power HardCopy III devices. Table 11–1 lists the external power supply pins for HardCopy III E devices. You can supply some of the power supply pins with the same external power supply, provided their supply voltage levels are the same.

For possible values of each power supply, refer to the *DC and Switching Characteristics of HardCopy III Devices* chapter.

Table 11–1. HardCopy III Power Supply Requirements (Part 1 of 2)

Power Supply Pin	Stratix III Voltage Value (V)	HardCopy III Voltage Value (V)	Description
VCCL *(1)*	0.9 / 1.1 (Selectable Core Voltage)	0.9	Core voltage power supply
VCC	1.1	0.9	I/O registers power supply
VCCIO	1.2 / 1.5 / 1.8 / 2.5 / 3.0 / 3.3	1.2 / 1.5 / 1.8 / 2.5 / 3.0 *(2)*	I/O power supply
VCCPGM	1.8 / 2.5 / 3.0 / 3.3	1.8 / 2.5 / 3.0	Configuration pins power supply
VCCPD *(3)*	2.5 / 3.0 /3.3	2.5 / 3.0	I/O pre-driver power supply
VCCA_PLL	2.5	2.5	PLL analog global power to the PLL regulator
VCCD_PLL	1.1	0.9	PLL digital global power supply
VCC_CLKIN	2.5	2.5	Differential clock input pins power supply (top and bottom I/O banks only)

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Table 11–1. HardCopy III Power Supply Requirements (Part 2 of 2)

Power Supply Pin	Stratix III Voltage Value (V)	HardCopy III Voltage Value (V)	Description
VCCBAT	2.5	— *(6)*	Battery back-up power supply for design security volatile key register
VCCPT	2.5	2.5	Power supply for the temperature sensing diode and power-on-reset (POR) *(4)*
V_{REF}	V_{REF} *(5)*	V_{REF}	Power supply for the voltage-referenced I/O standards
GND	GND	GND	Ground

Notes to Table 11–1:

(1) VCCL and VCC can be driven with the same voltage regulator when VCCL = VCC as required by the Stratix III device.
(2) HardCopy III devices do not support 3.3-V I/O standards.
(3) VCCPD can be either 2.5 V or 3.0 V. For a 3.0-V I/O standard, VCCPD = 3.0 V. For 2.5 V I/O standard and below, VCCPD = 2.5 V.
(4) In Stratix III devices, this power supply is also used for programmable power technology.
(5) There is one V_{REF} pin per I/O bank. You can use an external power supply or a resistor divider network to supply this voltage.
(6) This power pin can be disconnected or remain connected on the board.

3.3-V I/O Standard Support

The maximum I/O power supply voltage of Stratix III and HardCopy III devices is different due to unique process technologies. Stratix III devices support up to 3.3-V I/O voltage and HardCopy III devices support up to 3.0-V I/O voltage because of the long term reliability of 40 nm process technology. Therefore, HardCopy III devices do not support 3.3-V I/O standards such as 3.3-V LVTTL or 3.3-V LVCMOS.

For more information about 3.3-V I/O standards, refer to the *HardCopy III Device I/O Features* chapter.

Similarly, Stratix III devices that are prototyped for HardCopy III devices are limited in selection to 3.0-V power supplies. Even so, HardCopy III 3.0-V I/Os can still properly interface with 3.3-V external ports with little loss in noise margin, given similar input and output voltage electrical characteristics.

Supporting HardCopy III and Stratix III Power Supplies

The three core power rails in both Stratix III and HardCopy III devices are: V_{CC}, V_{CCL}, and V_{CCD_PLL}. For Stratix III devices, the V_{CC} and V_{CCD_PLL} core power rails can be powered by a 1.1-V source, and the V_{CCL} rail is powered by either 0.9-V or 1.1-V source. HardCopy III power rails, on the other hand, are all powered by a 0.9-V source.

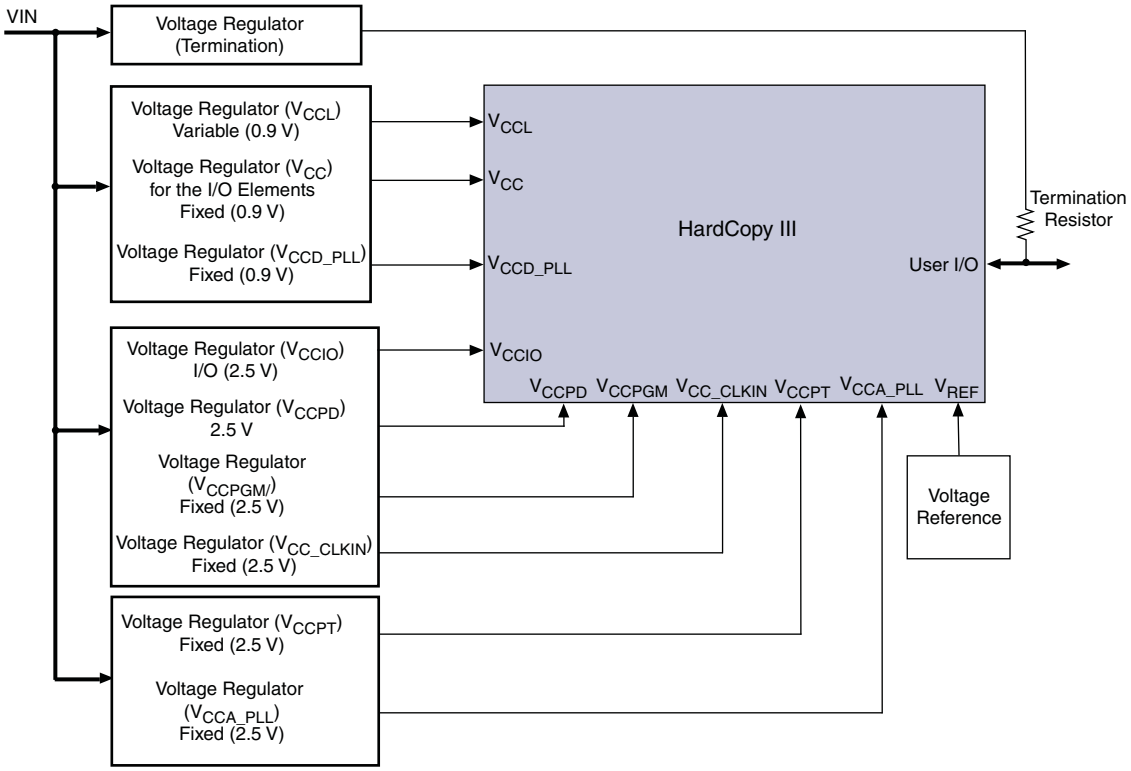
Table 11–2 shows the summary of core voltage requirements for these two devices.

Table 11–2. Core Voltage Requirements for Stratix III and HardCopy III Devices

Symbol	Parameter	Stratix III Devices	HardCopy III Devices	Unit
V_{CC}	I/O registers power supply	1.1	0.9	V
V_{CCL}	Core voltage supply	0.9/1.1 (Selectable Core Voltage)	0.9	V
V_{CCD_PLL}	PLL digital power supply	1.1	0.9	V

Stratix III-to-HardCopy III mapping requires all core voltages to be reduced from 1.1-V (for Stratix III devices) to 0.9-V (for HardCopy III devices). Therefore, you must select a voltage regulator that can support both voltages. For example, the Linear Technology LTC3713, National Semiconductor LM2743, and Texas Instrument TPS54610PWP support both 0.9-V and 1.1-V voltages. In most cases, you can simply change the feedback resistor values to adjust the output voltage of these regulators. Figure 11–1 shows an example of the power management of a HardCopy III device.

Figure 11–1. HardCopy III Power Management Example



For more information about these voltage regulator models, refer to materials at www.national.com, www.linear.com, and focus.ti.com.

HardCopy III Power Optimization

Because HardCopy III devices have lower power requirements than Stratix III devices, HardCopy III devices do not need either selectable core voltage or programmable power technology. Therefore, these options are not needed in HardCopy III devices. The Quartus® II software compiles your HardCopy III design according to the timing requirements specified in the timing constraint file. Due to smaller device geometry and optimized device architecture, HardCopy III devices generally achieve faster performance and lower power than Stratix III devices. The compilation reports show the power and performance of both the HardCopy III ASIC and the Stratix III FPGA.

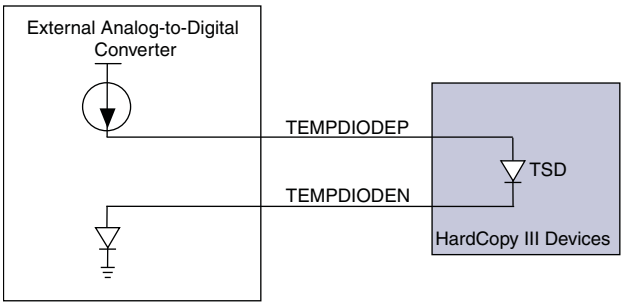
Temperature Sensing Diode (TSD)

The HardCopy III TSD uses the characteristics of a PN junction diode to determine die temperature. Knowing the junction temperature is crucial for thermal management. Junction temperature is calculated using ambient or case temperature, junction-to-ambient (θ_{JA}) or junction-to-case (θ_{JC}) thermal resistance, and the device power consumption. A HardCopy III device can monitor its die temperature with an embedded TSD, giving you control of the air flow to the device with external circuitry. Similar to Stratix III devices, you must use the HardCopy III device with an external analog-to-digital converter (ADC).

External Pin Connections

The HardCopy III TSD, located in the top-right corner of the die, requires two pins for voltage reference. You can connect the HardCopy III TSD with an external ADC converter. Figure 11–2 shows the TSD connections for HardCopy III devices.

Figure 11–2. TSD External Pin Connections in HardCopy III Devices



The TSD is a very sensitive circuit that can be influenced by noise coupled from other traces on the board and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on millivolts (mV) of difference, as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends taking temperature readings during periods of no activity in the device. If the TSD is not connected to an external temperature sense device, then connect the TSD pins to GND.

Document Revision History

Table 11–3 lists the revision history for this chapter.

Table 11–3. Document Revision History (Part 1 of 2)

Date	Version	Changes
January 2011	3.2	■ Changed chapter title. ■ Minor text edits.
January 2010	3.1	■ Modified Table 11–1. ■ Minor text edits.

Table 11–3. Document Revision History (Part 2 of 2)

Date	Version	Changes
June 2009	3.0	■ Updated Table 11–2 ■ Minor text edits
December 2008	2.0	■ Updated “External Pin Connections” on page 11–5. ■ Updated Figure 11–2. ■ Made minor editorial changes.
May 2008	1.0	Initial release.