CUSTOMER ADVISORY

ADV0039

Agilex™ 7 FPGA and SoC FPGA Known Issue List Document Updates

Issued: 06/08/2026

Description

Altera is notifying customers of updates to the Known Issue (KI) List for Agilex 7 F-Series, I-Series, and M-Series devices. Please go to the table below for the links to download the updated documents, and an overview of the key updates.

For a complete list, please review the revision history at the end of the KI document.

Agilex 7 F-Series and I- Series Known Issue List Document Download the document here: Agilex 7 F-/I-Series Known Issue List	
Section	**Updates Overview: R-Tile**
2.1.2.20	Added the R-tile PCIe Functional Failures After CvP Update known issue. **Knowledge Base Article** https://community.altera.com/kb/knowledge-base/why-are-there-pcie-functional-failures-observed-after-a-configuration-via-protoc/351910
Section	**Updates Overview: F-Tile**
2.1.1.27	Added: Receiver On-chip Termination Value Exceeds PCI Express Card Electromechanical Specification Guidelines. **Related Knowledge Base Article** Why is receiver termination reported as "Off" for the PCI Express* differential data pair in the Quartus® Prime Pro Edition software version 25.1.1 for design targeting Agilex™ 7 FPGA F-Tiles Devices?
2.1.1.28	Added: F-Tile FGT RX PCS may not be locked in OIF-CEI-56G-VSR-PAM4 or IEEE 802.3-2022 200GAUI-4 C2M/400GAUI-8 C2M modes during power up and reset release known issue
2.1.1.29	Added: FGT FW may use an invalid CTLE offset code (maximum correction) during the initial boot, instead of using the calibrated value. This can lead to sub-optimal RX equalization. RX PCS may not be locked known issue
2.1.1.31	Added: F-Tile FGT Design with Fractional PLL may transmit TX data at an incorrect rate after simultaneous TX & RX Resets. No impact for TX PLL in integer mode known issue

2.1.1.32	Added: PCS ready assertion may be delayed for 50G PAM4 MR protocols without ANLT (approximately 10-13 dB IL) due to sub-optimal convergence and requires additional calibration known issue
2.1.1.30	Added: FHT 112G OIF/CEI VSR & MR compliance require firmware update known issue
2.1.1.33	Added: FHT AN/LT suboptimal TX equalization convergence when calibrated below 0°C leading to 400G/200G/100G IEEE CR/KR with AN/LT non-compliance at higher temperatures known issue

Agilex 7 M-Series Known Issue List Document Download the document here: Agilex 7 M-Series Known Issue List	
Section	**Updates Overview: R-Tile**
2.1.2.12.	Added the R-tile PCIe Functional Failures After CvP Update known issue **Knowledge Base Article** https://community.altera.com/kb/knowledge-base/why-are-there-pcie-functional-failures-observed-after-a-configuration-via-protoc/351910
Section	**Updates Overview: F-Tile**
2.1.1.23	Added: Receiver On-chip Termination Value Exceeds PCI Express Card Electromechanical Specification Guidelines **Related Knowledge Base Article** Why is receiver termination reported as "Off" for the PCI Express* differential data pair in the Quartus® Prime Pro Edition software version 25.1.1 for design targeting Agilex™ 7 FPGA F-Tiles Devices?
2.1.1.24	Added: F-Tile FGT RX PCS may not be locked in OIF-CEI-56G-VSR-PAM4 or IEEE 802.3-2022 200GAUI-4 C2M/400GAUI-8 C2M modes during power up and reset release known issue
2.1.1.25	Added: FGT FW may use an invalid CTLE offset code (maximum correction) during the initial boot, instead of using the calibrated value. This can lead to sub-optimal RX equalization. RX PCS may not be locked known issue
2.1.1.27	Added: F-Tile FGT Design with Fractional PLL may transmit TX data at an incorrect rate after simultaneous TX & RX Resets. No impact for TX PLL in integer mode known issue

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2.1.1.28	Added: PCS ready assertion may be delayed for 50G PAM4 MR protocols without ANLT (approximately 10-13 dB IL) due to sub-optimal convergence and requires additional calibration known issue
2.1.1.26	Added: FHT 112G OIF/CEI VSR & MR compliance require firmware update known issue
2.1.1.29	Added: FHT AN/LT suboptimal TX equalization convergence when calibrated below 0°C leading to 400G/200G/100G IEEE CR/KR with AN/LT non-compliance at higher temperatures known issue

Recommended Actions

Customers are requested to review the change and determine the impact on their designs.

Specific impacted part numbers will depend on the issue. To assist with the review, you may refer to the ordering part numbers (OPNs) list showing the product series, tile, and Hard Processor System (HPS) status information (see link on the Products Affected section).

Products Affected

Agilex 7 F-Series, I-Series, M-Series

The list of the ordering part numbers (OPNs) can be downloaded in Excel form here:

https://docs.altera.com/v/u/resources/r604031/part-number-list-for-adv0039

Specific impacted part numbers will depend on the issue. To assist with the review, you may refer to the added columns indicating the product series, tile, and Hard Processor System (HPS) status information on the OPN list.

Contact

For more information, please contact your local Sales/FAE representative, distributor, or submit a support ticket at Altera Premier Support (APS).

Customer Notifications Subscription

Altera publishes customer notifications (PCN/PDN/ADV) on altera.com at the Quality &

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Reliability page.

To be notified of new customer notifications, here are the steps: 1) log in to myaltera; 2) click or load this PCN/ADV/PDN Collection link; 3) click on "save search" on the upper right; 4) enter a name for this search; 5) click on "Activate alert" box; 6) click "Save".

Revision History

Date	Rev	Description
05/21/2026	1.0	Initial Release
05/26/2026	2.0	Corrected the KDB link for issue on section 2.1.1.27 of Agilex 7 F-Series and I- Series Known Issue List table and section 2.1.1.23 of Agilex 7 M-Series Known Issue List table.
06/08/2026	3.0	Updated the statement to match title of KI document issue on section 2.1.1.27 of Agilex 7 F-Series and I-Series Known Issue List table and section 2.1.1.23 of Agilex 7 M-Series Known Issue List table.

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