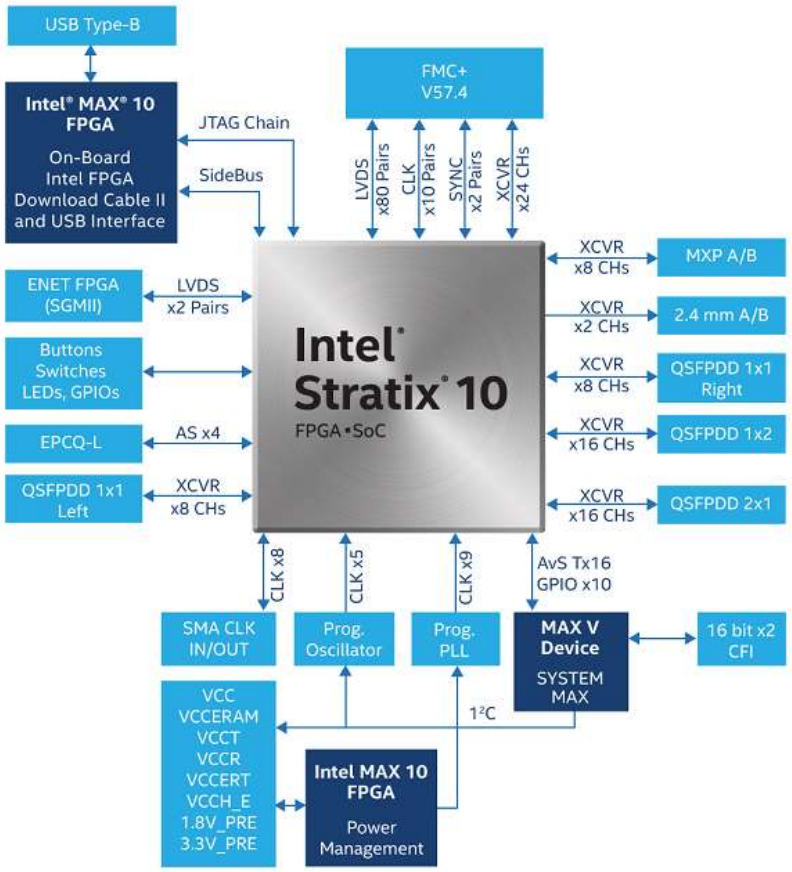
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321330-B
Gerber Files	110-0321330-B
PCB Design Files	120-0321330-B
Assembly Drawing	130-0321330-B
Fab Drawing	140-0321330-B
Schematic Drawing	150-0321330-B
PCB Film	160-0321330-B
Bill of Materials	170-0321330-B
Schematic Design Files	180-0321330-B
Functional Specification	210-0321330-B
PCB Layout Guidelines	220-0321330-B
Assembly Rework	320-0321330-B

Stratix 10 TX SI Development Kit



REV	DATE	PAGES	DESCRIPTION
A0	5 June. 2017	All	INITIAL REVISION A RELEASE
A1	11 Sep. 2017	All	A1 REVISION A RELEASE, refer to page 53 for change list
A2	1 Nov. 2017	All	A2 REVISION A RELEASE, refer to Page 53 for change list
B1	1 Jan. 2019	All	B1 REVISION B RELEASE, refer to Page 53 for change list

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History	30	S10 Bottom Banks - 3A/B/C
2	Power Tree	31	S10 HTile Banks - 1C/D/E/F
3	Clock Tree, Bank Usage	32	S10 ETile Banks - 8B
4	I2C Chain	33	S10 ETile Banks - 8C
5	JTAG Chain	34	S10 ETile Banks - 9A
6	Clock 1	35	S10 ETile Banks - 9B
7	Clock 2	36	S10 ETile Banks - 9C
8	On Board USB BLASTER II 1	37	S10 PWR
9	On Board USB BLASTER II 2	38	S10 GND
10	MAX10 PWR Manager 1	39	PWR - POWER INPUT
11	MAX10 PWR Manager 2	40	PWR - VCC 1
12	Temperature Sense/FAN	41	PWR - VCC 2
13	SYSMAX	42	PWR - VCCERAM
14	NA	43	PWR - VCCT/VCCR
15	CFI Flash Memory	44	PWR - VCCERT
16	10/100/1000 Ethernet PHY	45	PWR - VCCH_E/1.8V_PRE
17	Buttons/Switches/LEDs	46	PWR - 3.3V_PRE
18	Level shifter/Buffer	47	PWR - 5V
19	NA	48	PWR - S10_1V8&2V5/2V4
20	QSFPDD 1x1 Right	49	PWR - IO_2V5&3V3&12V
21	QSFPDD 1x1 Left	50	Decoupling 1
22	QSFPDD 1x2	51	Decoupling 2
23	QSFPDD 2x1	52	Fast Discharge and V-Sense
24	NA	53	Revision History
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26	FMC+ 1	55	
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29	S10 Top Banks 2 L/M/N	58	

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FPGA Power UP Sequencing:

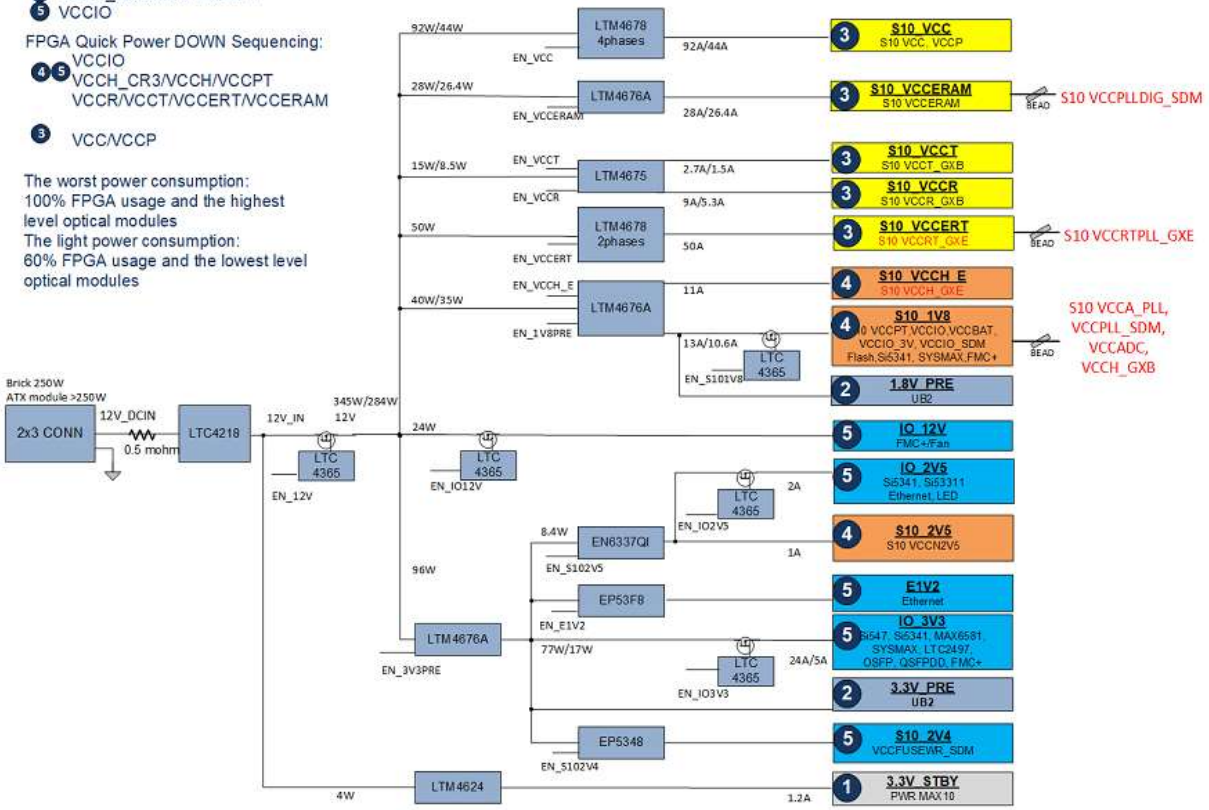
3 VCC/VCCP/VCCERAM
VCCR/VCCT/VCCERT
4 VCCH_CR3/VCCH/VCCPT
5 VCCIO

FPGA Quick Power DOWN Sequencing:

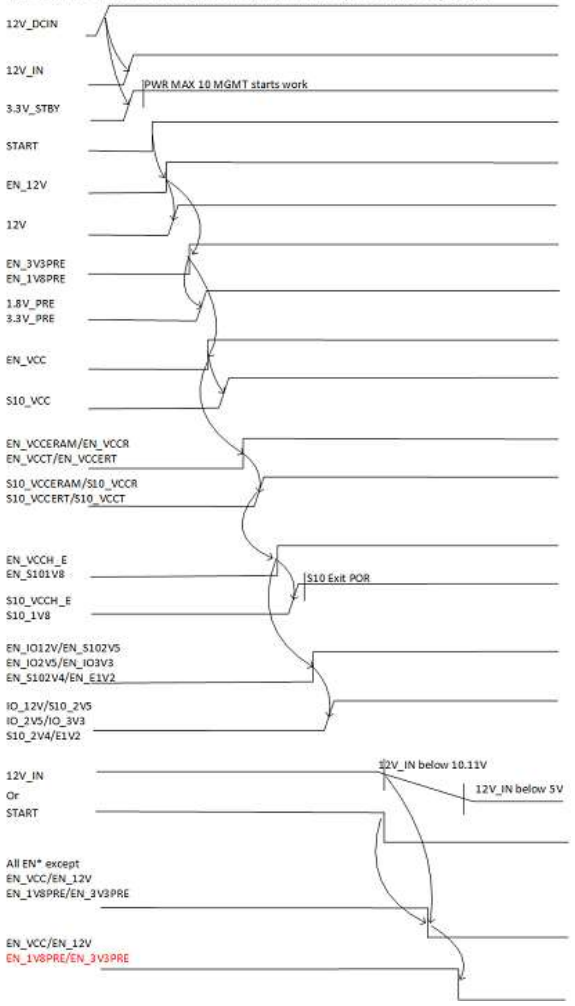
4 5 VCCIO
VCCH_CR3/VCCH/VCCPT
VCCR/VCCT/VCCERT/VCCERAM

3 VCC/VCCP

The worst power consumption:
100% FPGA usage and the highest level optical modules
The light power consumption:
60% FPGA usage and the lowest level optical modules



Stratix 10 TX SI Development Kit Power Up/Down Sequence



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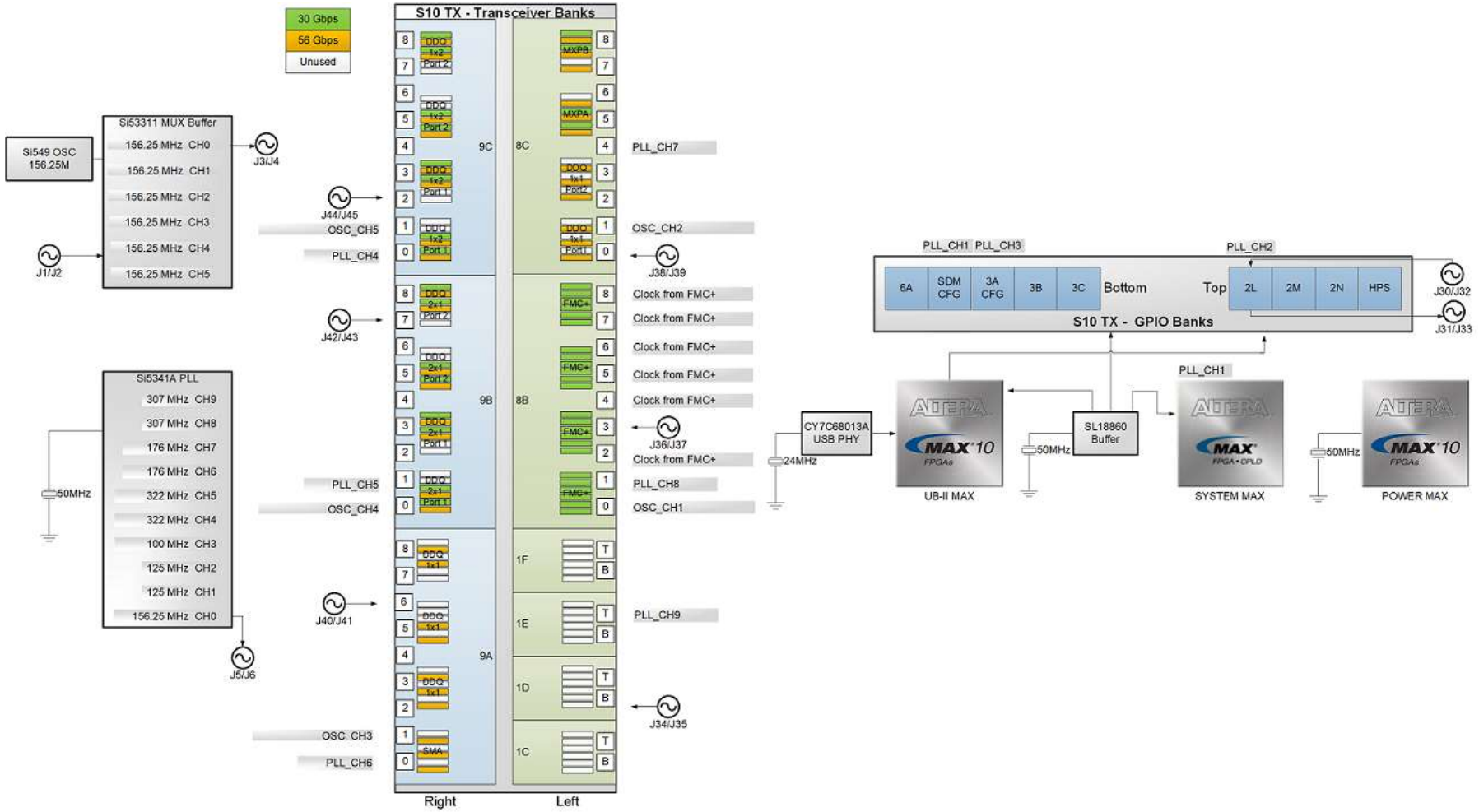
Clock Tree, Bank Usage



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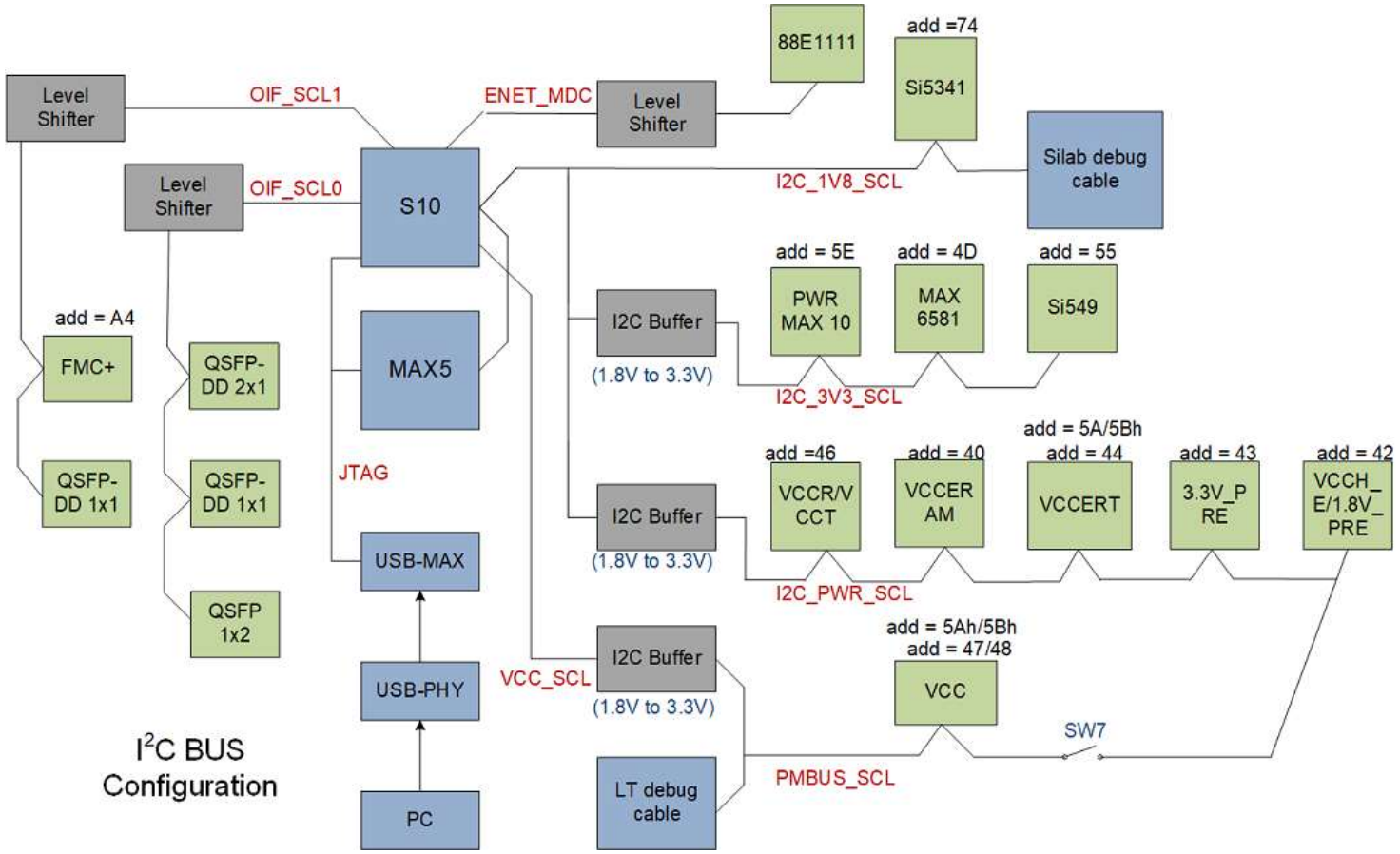
I2C Chains



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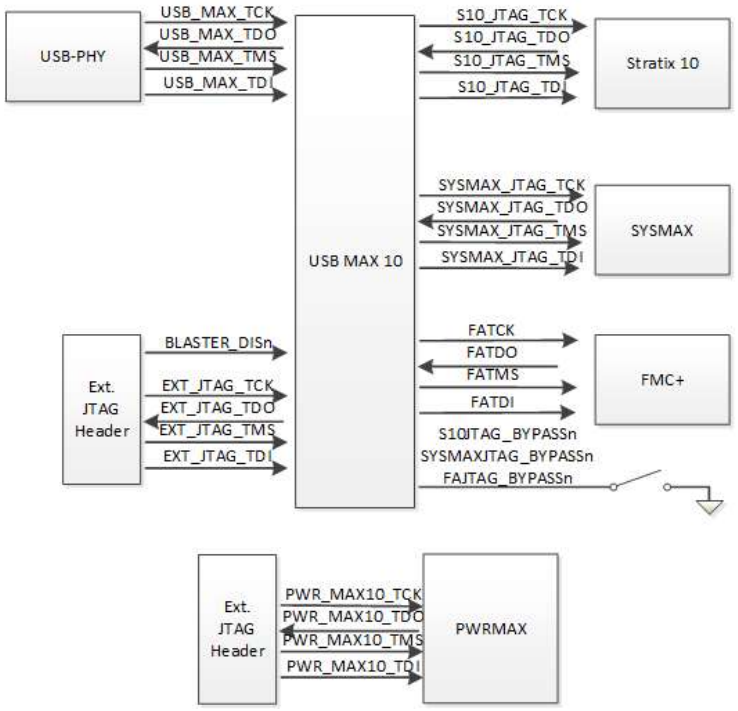
JTAG Chain



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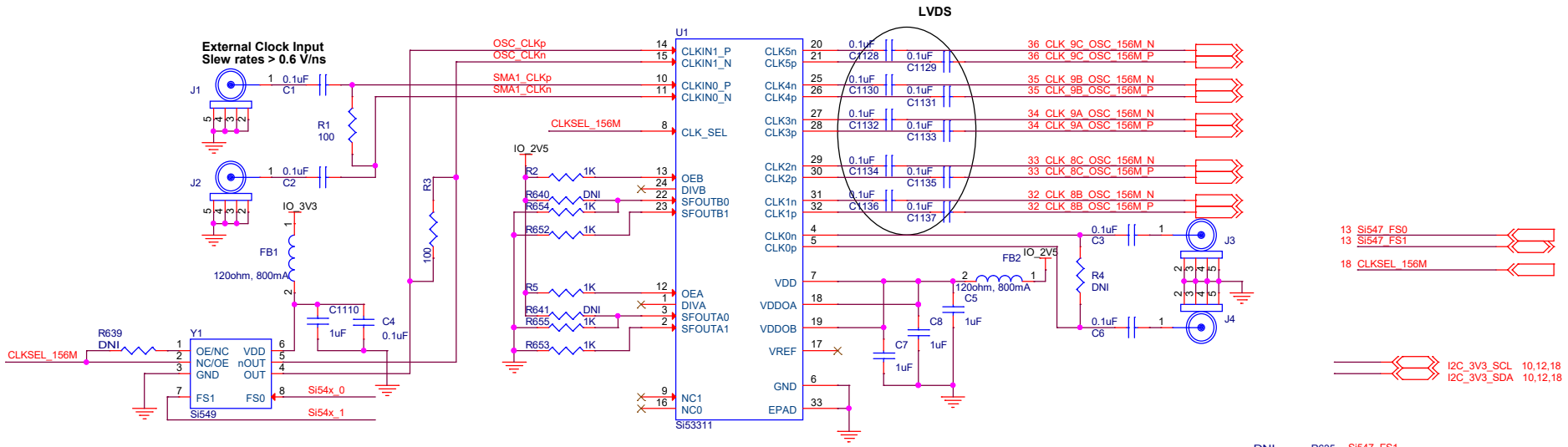
Clock 1



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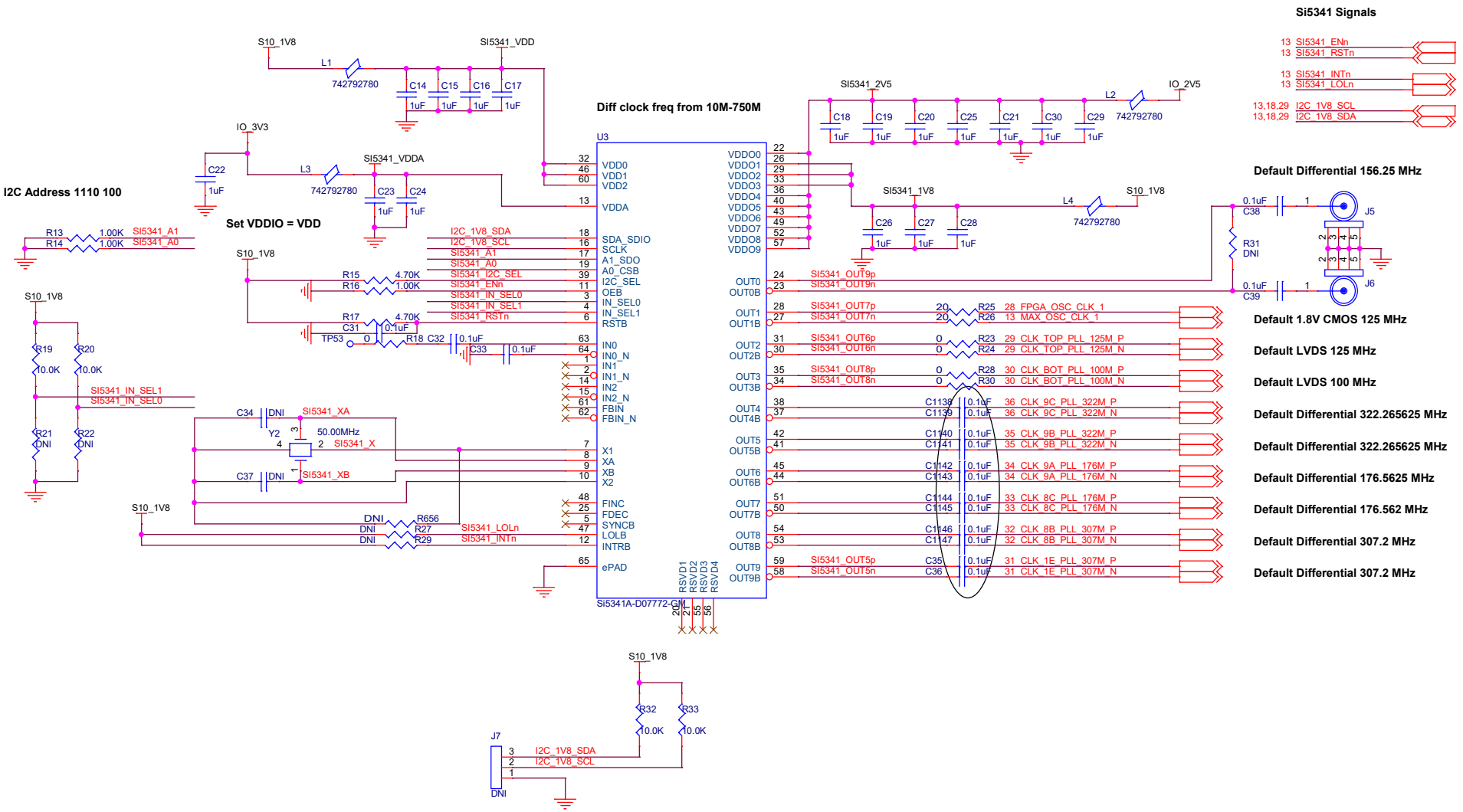
Clock 2



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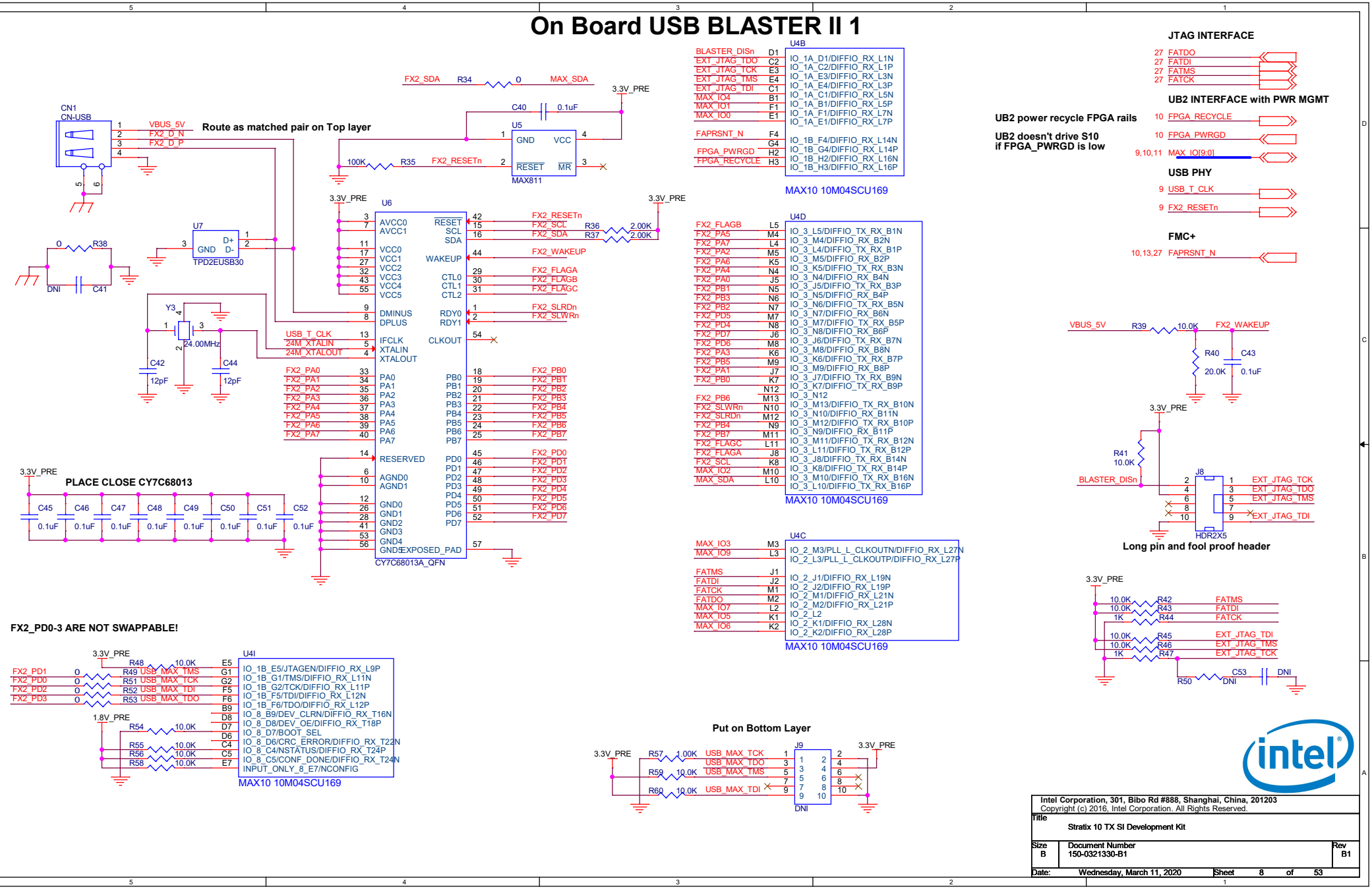
On Board USB BLASTER II 1



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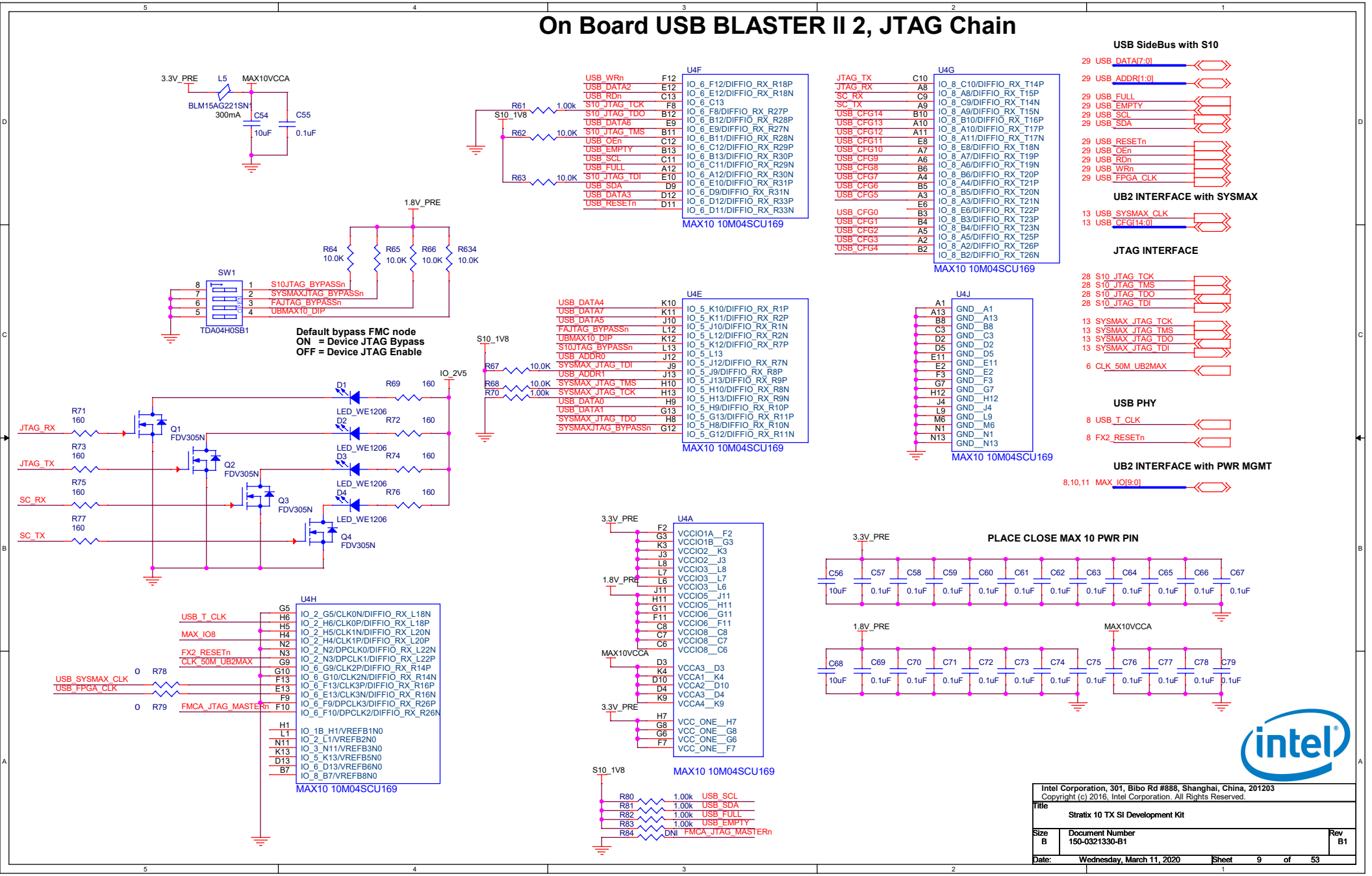
On Board USB BLASTER II 2, JTAG Chain



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MAX 10 PWR Manager 1

Monitor Non-Digital Rails
1: IO_2V5
2: IO_3V3
3: ETHE_1V2
4: 2V4
5: S10_2V5
6: S10_1V8
7: 12V
8: IO_12V
9: 12V_IN

Slave Address 0101 111

Power down system as FPGA temperature alert

Reset FPGA by nCONFIG as power down start

POWER GOOD: VCC,VCCERAM,VCCT,VCCR,VCCH_E,VCCERT, 12V_IN,1V8_PRE,3V3_PRE,IO_2V5,E1V2,FMC,12V,IO_12V

UB2/PWR MGMT INTERFACE

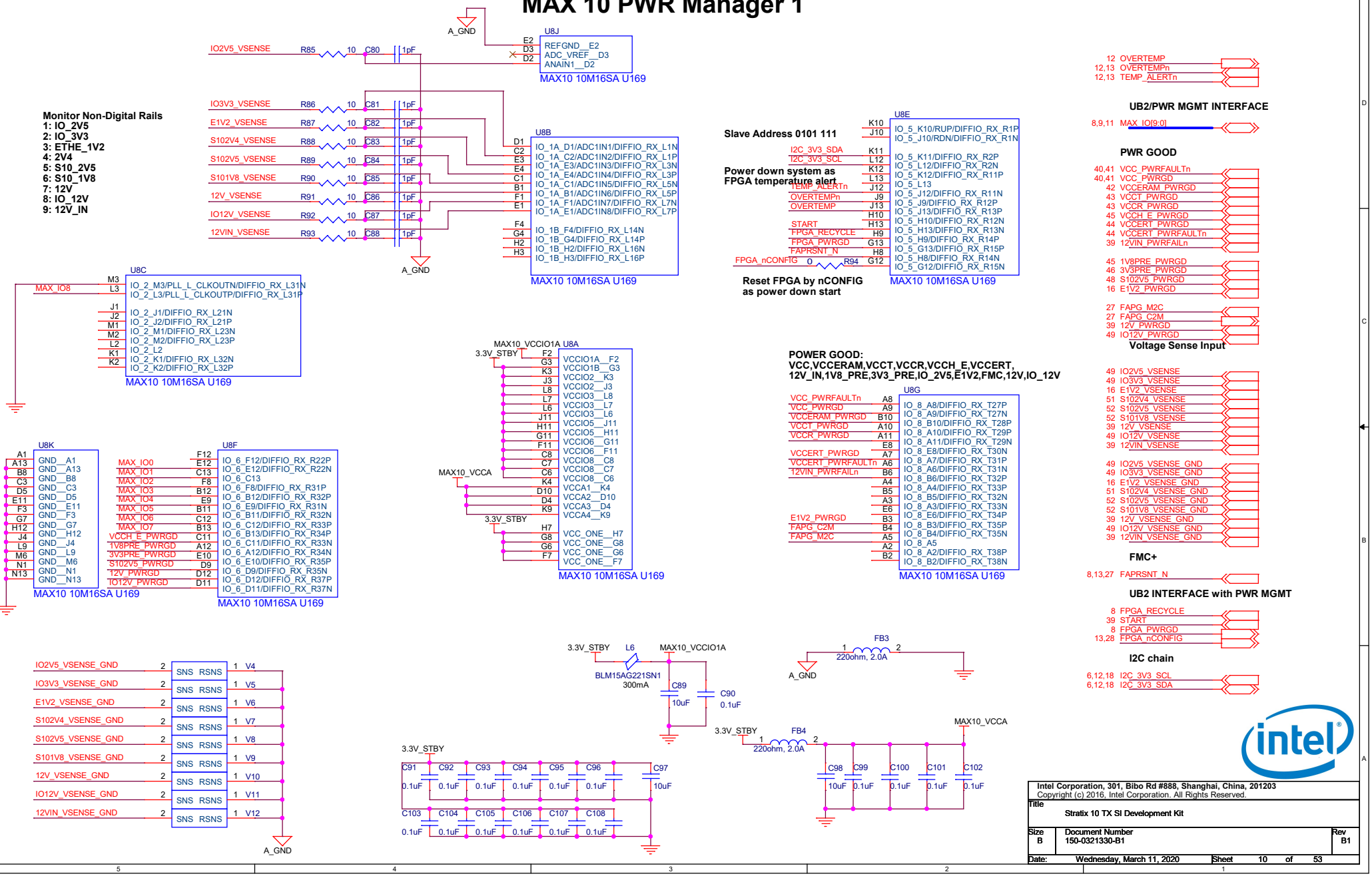
PWR GOOD

Voltage Sense Input

FMC+

UB2 INTERFACE with PWR MGMT

I2C chain



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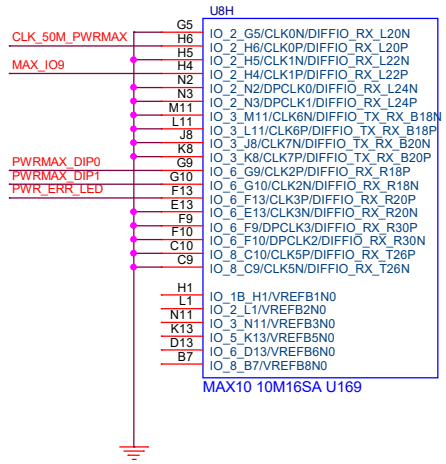
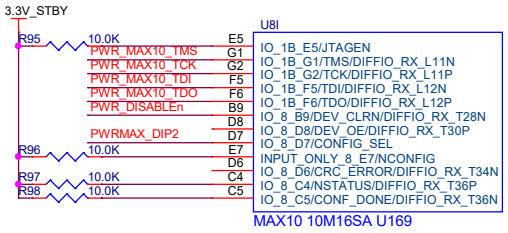
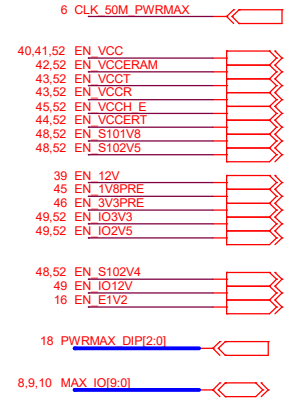
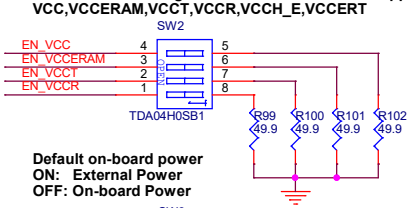
MAX10 PWR Manager 2



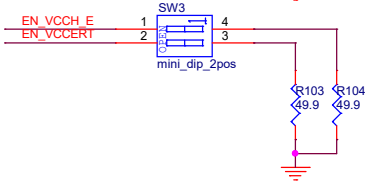


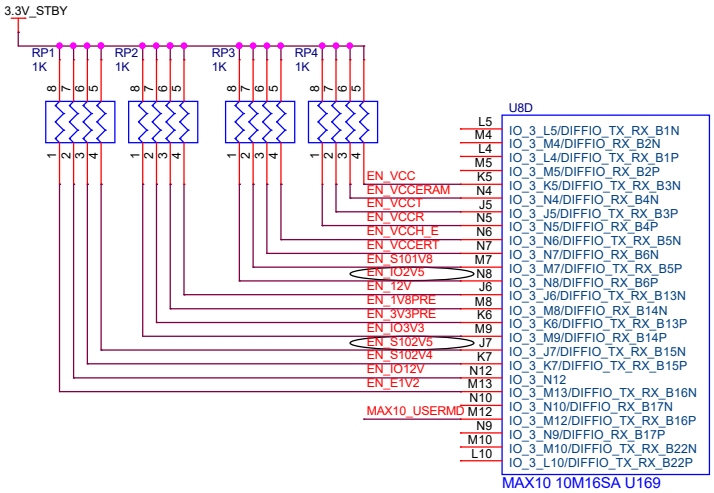


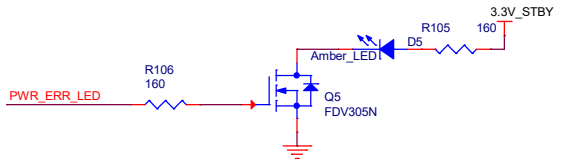
Disable on-board regulator before use external supply:
VCC,VCCERAM,VCCT,VCCR,VCCH_E,VCCERT



Default on-board power
ON: External Power
OFF: On-board Power

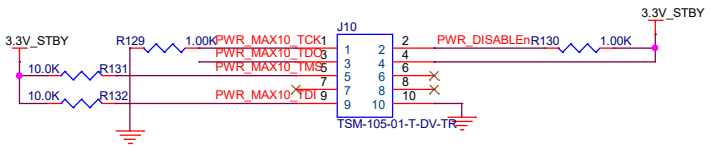


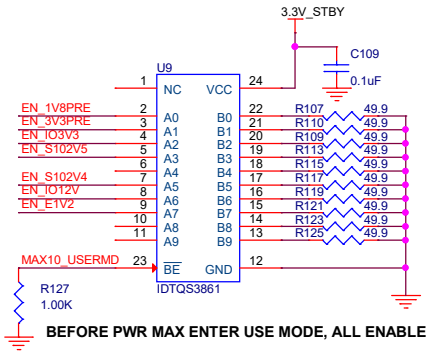


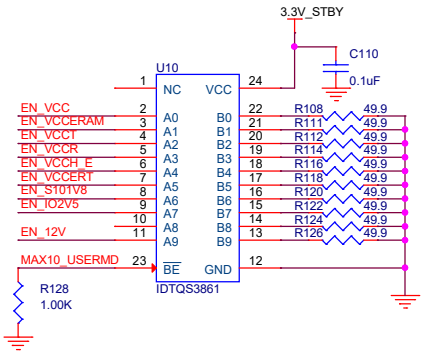


VCC,VCCERAM,VCCT,VCCR,VCCH_E,VCCERT,S10_1V8,S10_2V5
12V,1V8PRE,3V3PRE,IO3V3,IO2V5,S102V4,IO12V

Put on Bottom Layer
PWRMAX enter debug mode and all rails are sequence off if PWR_DISABLEn is low







BEFORE PWR MAX ENTER USE MODE, ALL ENABLE are LOW

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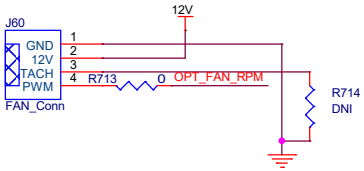
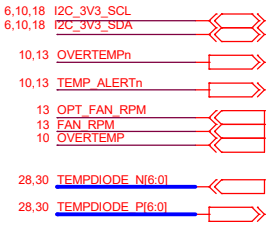
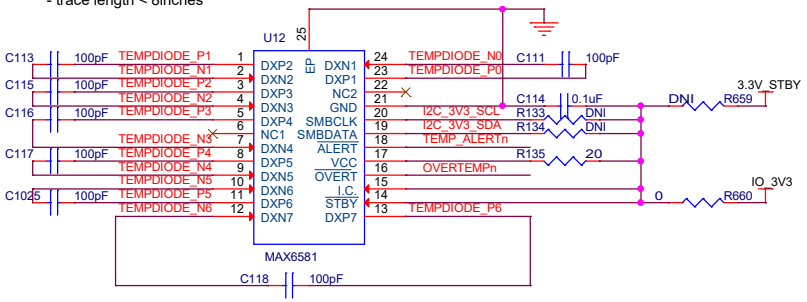
Temperature Sense/FAN





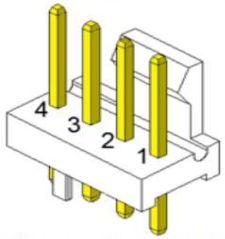
Note: TEMPDIODE instructions
- route as diff pair and less vias
- use GND guard traces
- trace width = 10mils
- trace gap = as minimum as possible
- trace length < 8inches

SLAVE ADDR = 1001 101



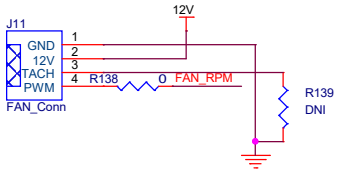
0: Core or SDM
1: 8B
2: 8C
3: 9A
4: 9B
5: 9C
6: 1C/D/E/F

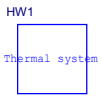
4-Wire Pulse Width Modulation (PWM) Controlled Fans



Motherboard CPU Fan 4 Pin header Connector.

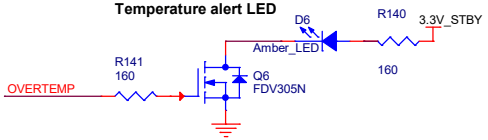
Pin	Name	Color
1	GND	black
2	+12VDC	yellow
3	Sense	green
4	Control	blue





Liquid Cooling system

Temperature alert LED



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SYSTEM MAX

FMC+

PCIe_PERSTn_1V8 30
FACLKDIR 27
FAPRSNT_N 8,10,27
PCIe_PERSTn_3V3 26
PCIe_WAKEn_3V3 26

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PMBUS_ALERTn 18,40,41
I2C_PWR_ALERTn 18,42,43,44,45,46
VCC_ALERTn 28
EN_MASTER[2:0] 18

UB2/FPGA INTERFACE with SYSMAX

CLK_50M_SYSMAX 6
USB_CFG[14:0] 9
USER_IO[9:0] 17,29
FAN_RPM 12
OPT_FAN_RPM 12

FPGA Configuration

FPGA_INIT_DONE 28
FPGA_nSTATUS 28
FPGA_CONF_DONE 28
FPGA_nCONFIG 10,28
FPGA_SEU_ERR 28
FPGA_CvP_DONE 28
FPGA_PR_REQUEST 30
FPGA_PR_DONE 30
FPGA_PR_ERROR 30
FPGA_MSEL[2:0] 28
FPGA_CONFIG_D[15:0] 30
FPGA_AVST_CLK 30
FPGA_AVST_VALID 30
FPGA_AVST_READY 28

FLASH Interface

FM_D[15:0] 15
FM_A[26:1] 15
FLASH_WEn 15
FLASH_CEn0 15
FLASH_CEn1 15
FLASH_OEn 15
FM_A27 15
FLASH_RDYBSYn 15
FLASH_RESETn 15
FLASH_WPn 15
FLASH_BYTEn 15

Temperature Interface

TEMP_ALERTn 10,12
OVERTEMPn 10,12
TEMP_ALERTn_1V8 29
OVERTEMPn_1V8 29

Clock

USB_SYSMAX_CLK 9
MAX_OSC_CLK_1 7

MAX5 JTAG

SYSMAX_JTAG_TDO 9
SYSMAX_JTAG_TDI 9
SYSMAX_JTAG_TCK 9
SYSMAX_JTAG_TMS 9

MAX5 Push Button

PGM_SEL 17
PGM_CONFIG 17
MAX_RESETn 17
CPU_RESETn 17,29

MAX5 Dipswitch

FACTORY_LOAD 17
MAX5_SWITCH[2:0] 17

MAX5 LED

PGM_LED[2:0] 17
MAX_ERROR 17
MAX_LOAD 17
MAX_CONF_DONE 17

MAX V I2C Master

I2C_1V8_SCL 7,18,29
I2C_1V8_SDA 7,18,29

Clock

SI5341_ENn 7
SI5341_RSTn 7
SI5341_INTn 7
SI5341_LOLn 7
SI547_FS0 6
SI547_FS1 6

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NA

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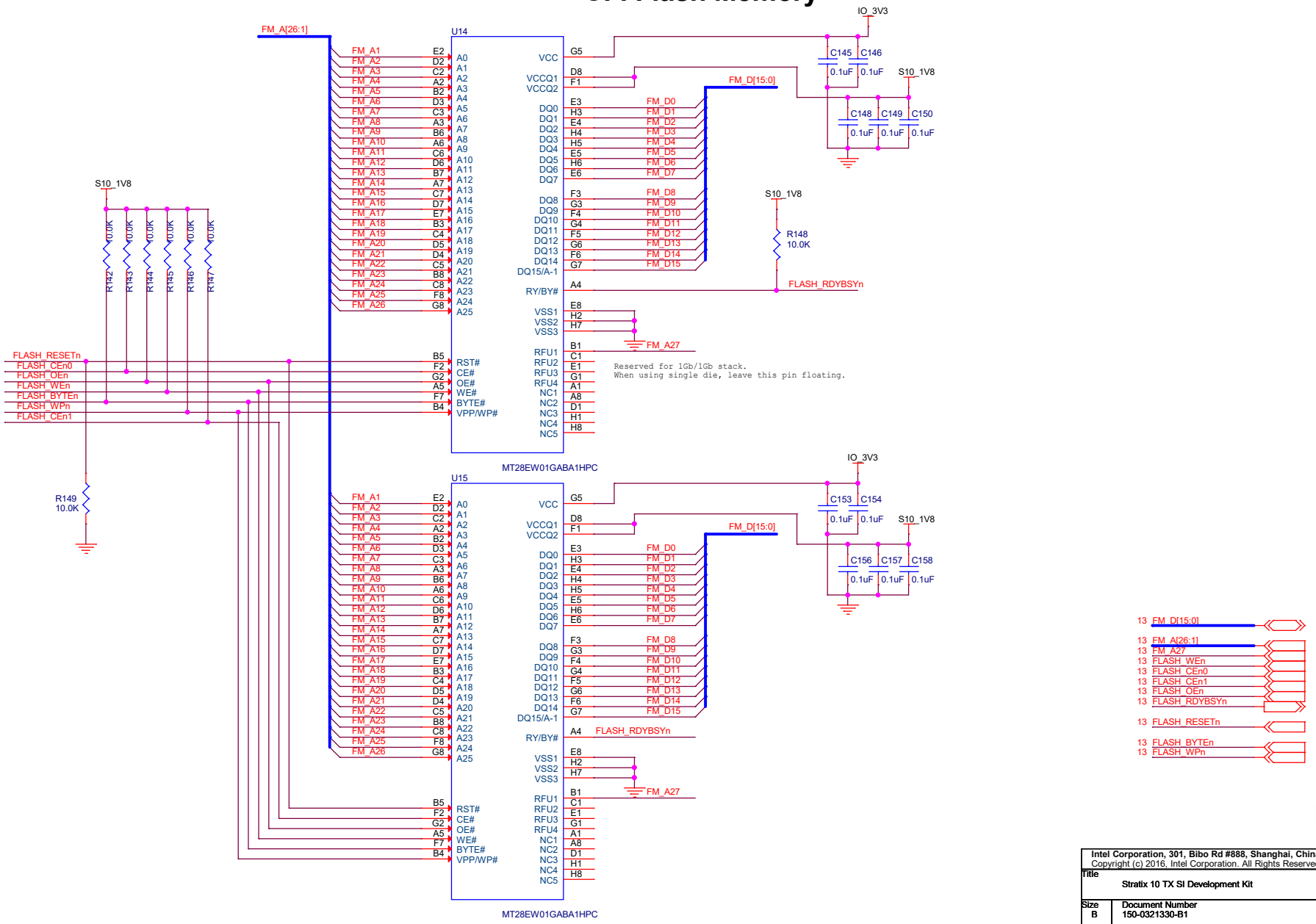
CFI Flash Memory



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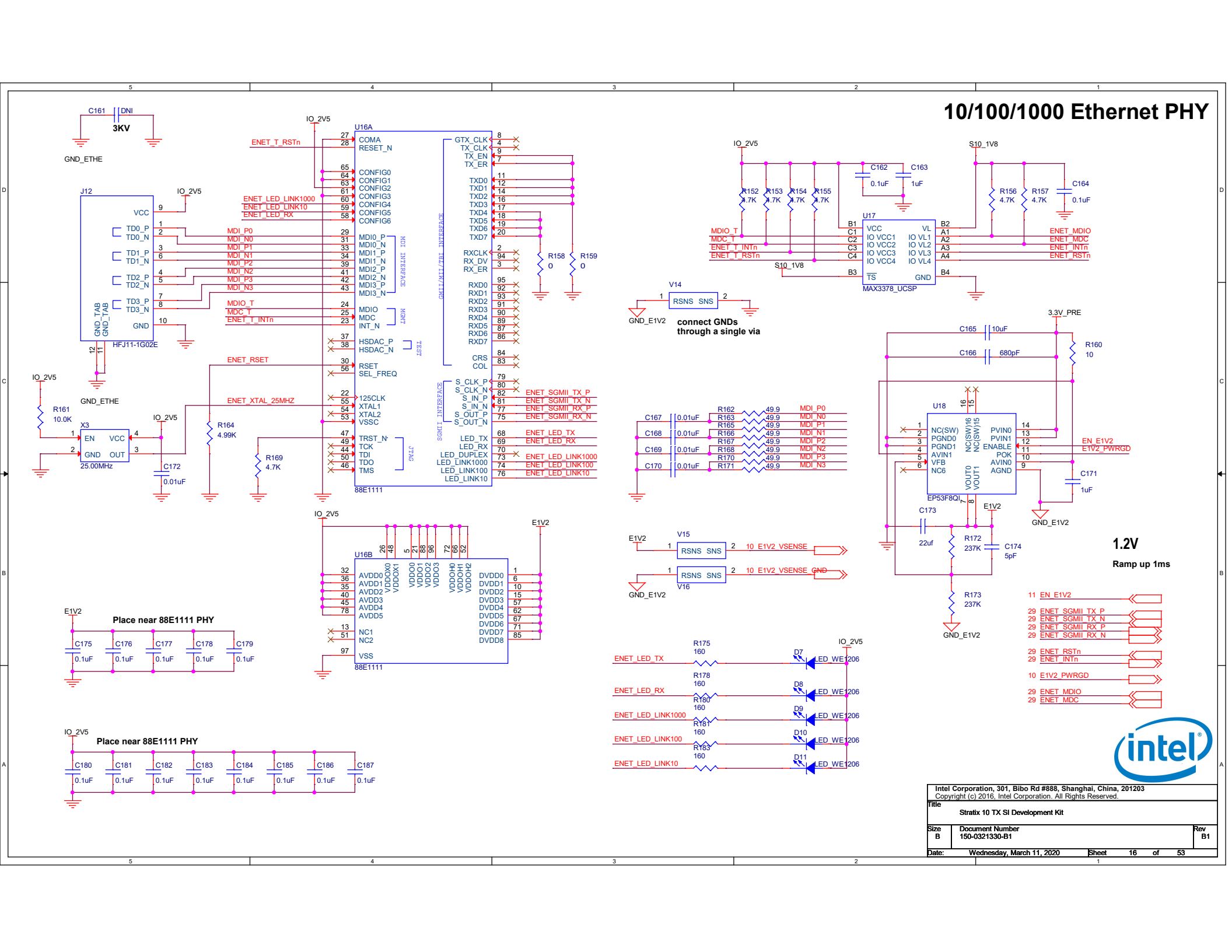
10/100/1000 Ethernet PHY



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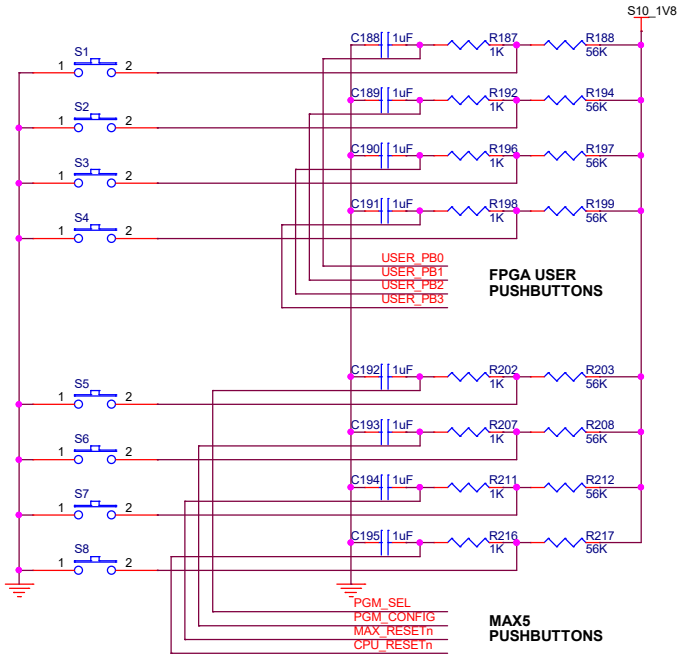
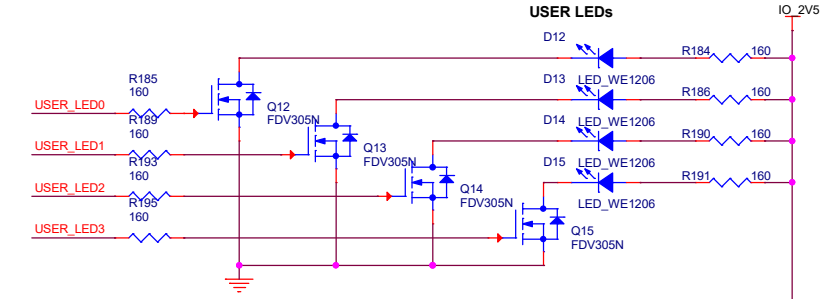
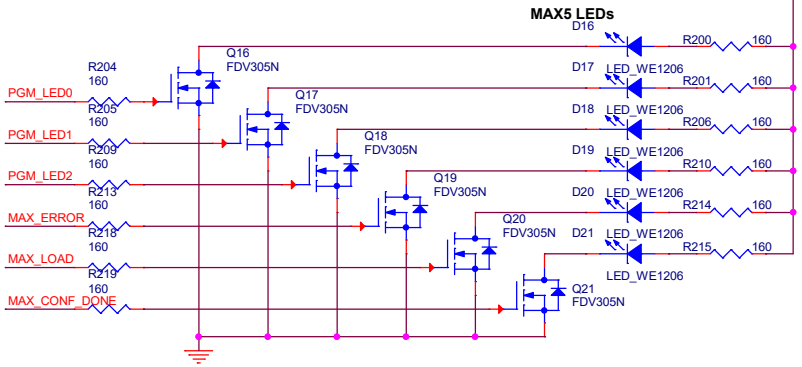
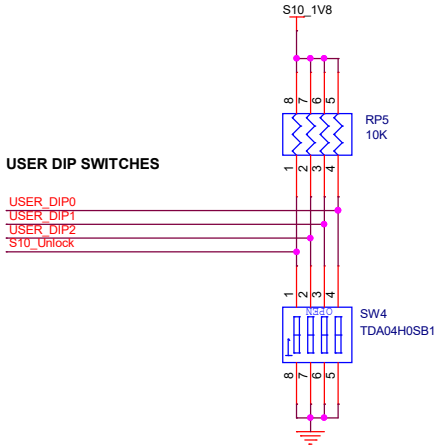
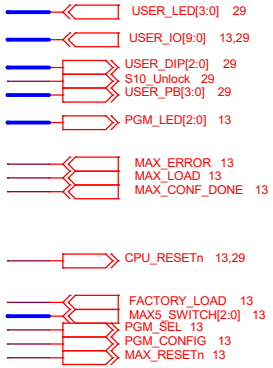
Buttons/Switches/LEDs

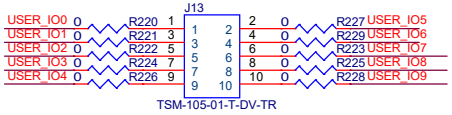


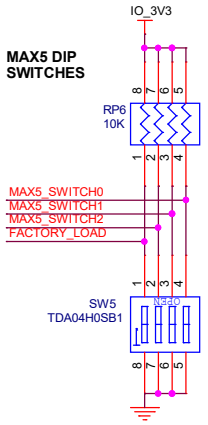












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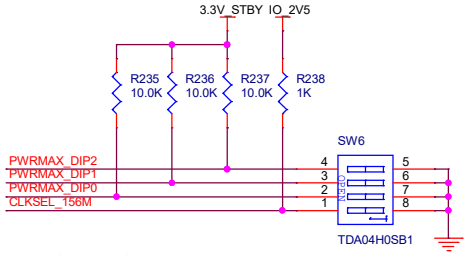
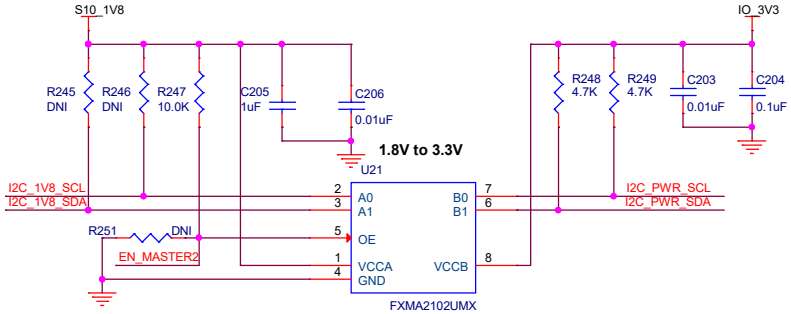
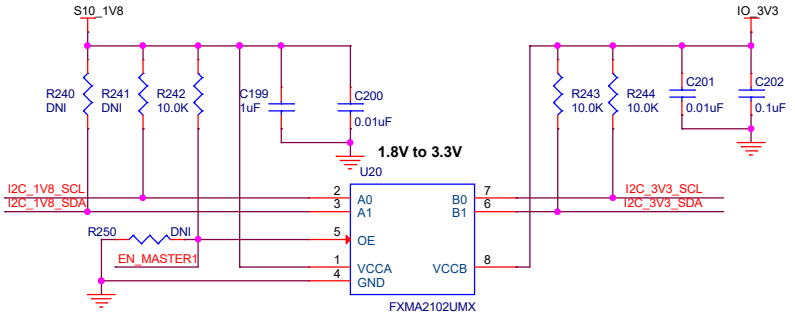
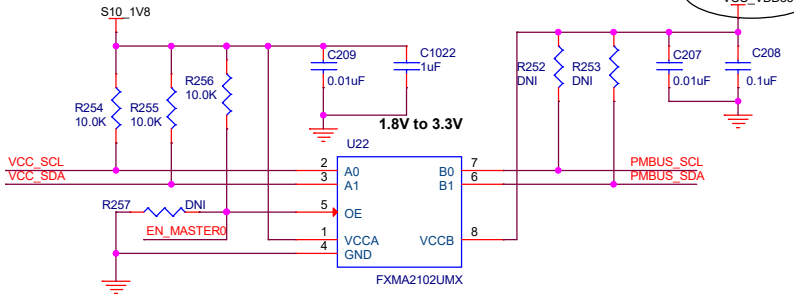
Level shifter/Buffer



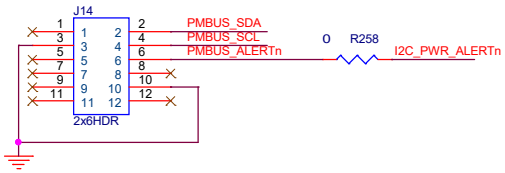
Bit 1 default OFF for Si570 source
OFF: Si570 is source
ON: SMA is source

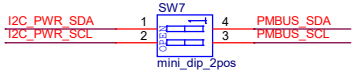






LT I2C Connector





Isolate VCC regulator from system I2C bus:
Default ON position for full chain.
OFF = VCC regulator ISOLATED
ON = FULL CHAIN

I2C BUS

I2C_1V8_SCL 7,13,29
I2C_1V8_SDA 7,13,29

I2C_3V3_SCL 6,10,12
I2C_3V3_SDA 6,10,12

EN_MASTER[2:0] 13
CLKSEL_156M 6
PWRMAX_DIP[2:0] 11

PMBUS_SCL 40,41
PMBUS_SDA 40,41
PMBUS_ALERTn 13,40,41

VCC_SCL 28
VCC_SDA 28

I2C_PWR_SDA 42,43,44,45,46
I2C_PWR_SCL 42,43,44,45,46

I2C_PWR_ALERTn 13,42,43,44,45,46

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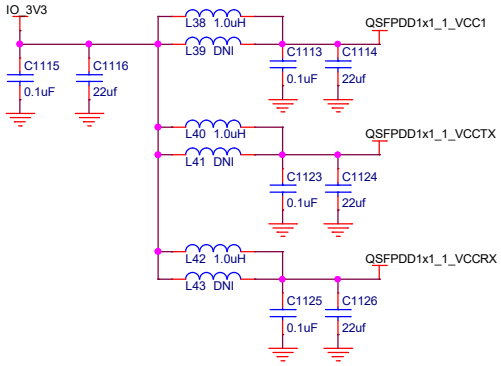
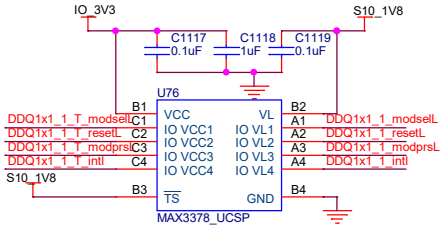
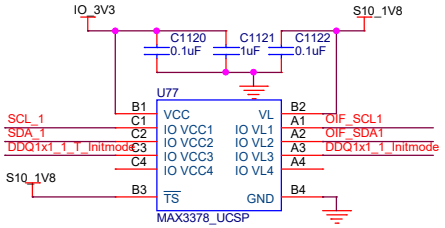
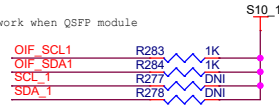
QSFPDD 1x1 Right

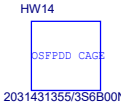






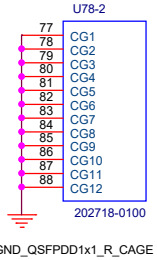
QSFPDD cage can support both QSFPDD and QSFP modules. The low four channels work when QSFP module is used. All eight channels work when QSFPDD module is plugged.



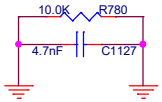


2031431355/3S6B00N-11401-4F

Molex/Fit-FoxCONN
CONN - 1x1 QSFP DD CAGE ASSEMBLY



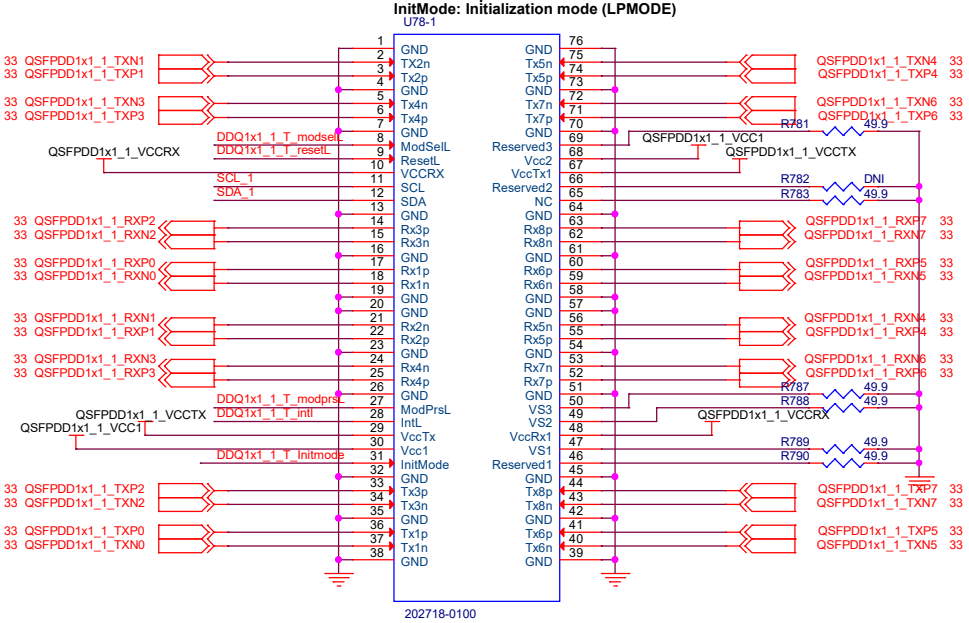
GND_QSFPDD1x1_R_CAGE

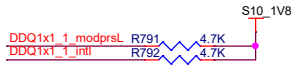


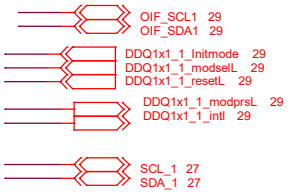
GND_QSFPDD1x1_R_CAGE

Cage GND on top layer

ModSelL: Module Select
ResetL: Module Reset
ModPrsL: Module Present
IntL: Interrupt
InitMode: Initialization mode (LPMODE)







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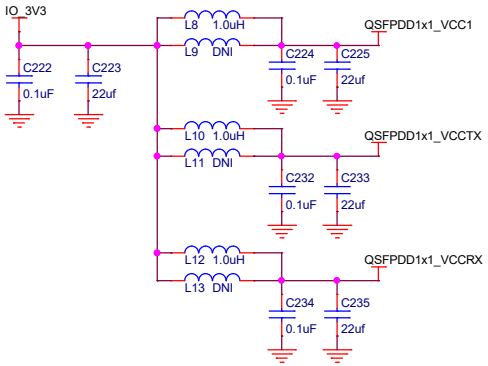
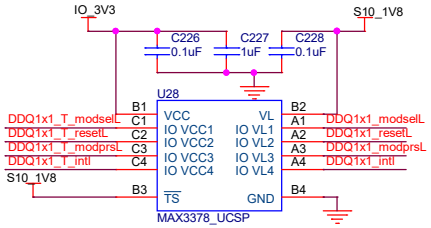
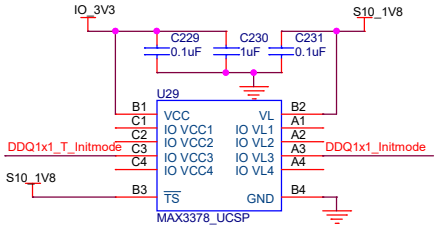
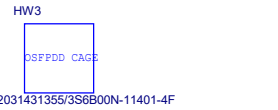
QSFPDD 1x1 Left



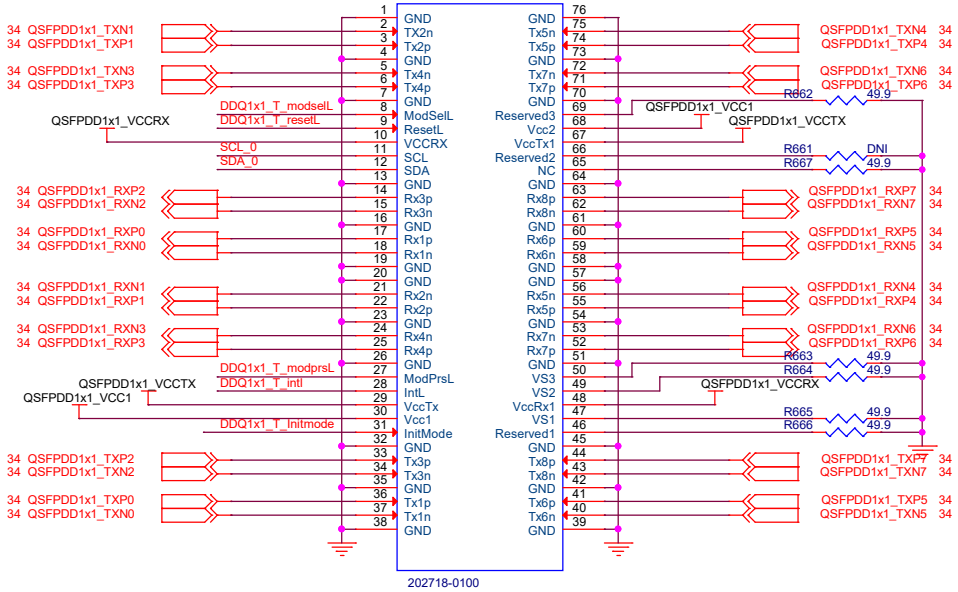


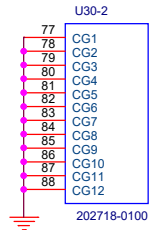


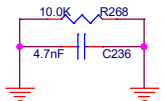
QSFPDD cage can support both QSFPDD and QSFP modules. The low four channels work when QSFP module is used. All eight channels work when QSFPDD module is plugged.



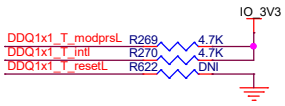
ModSelL: Module Select
ResetL: Module Reset
ModPrsL: Module Present
IntL: Interrupt
InitMode: Initialization mode (LPMODE)

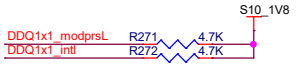


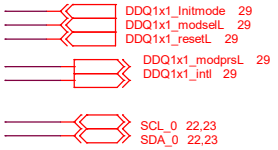




Cage GND on top layer







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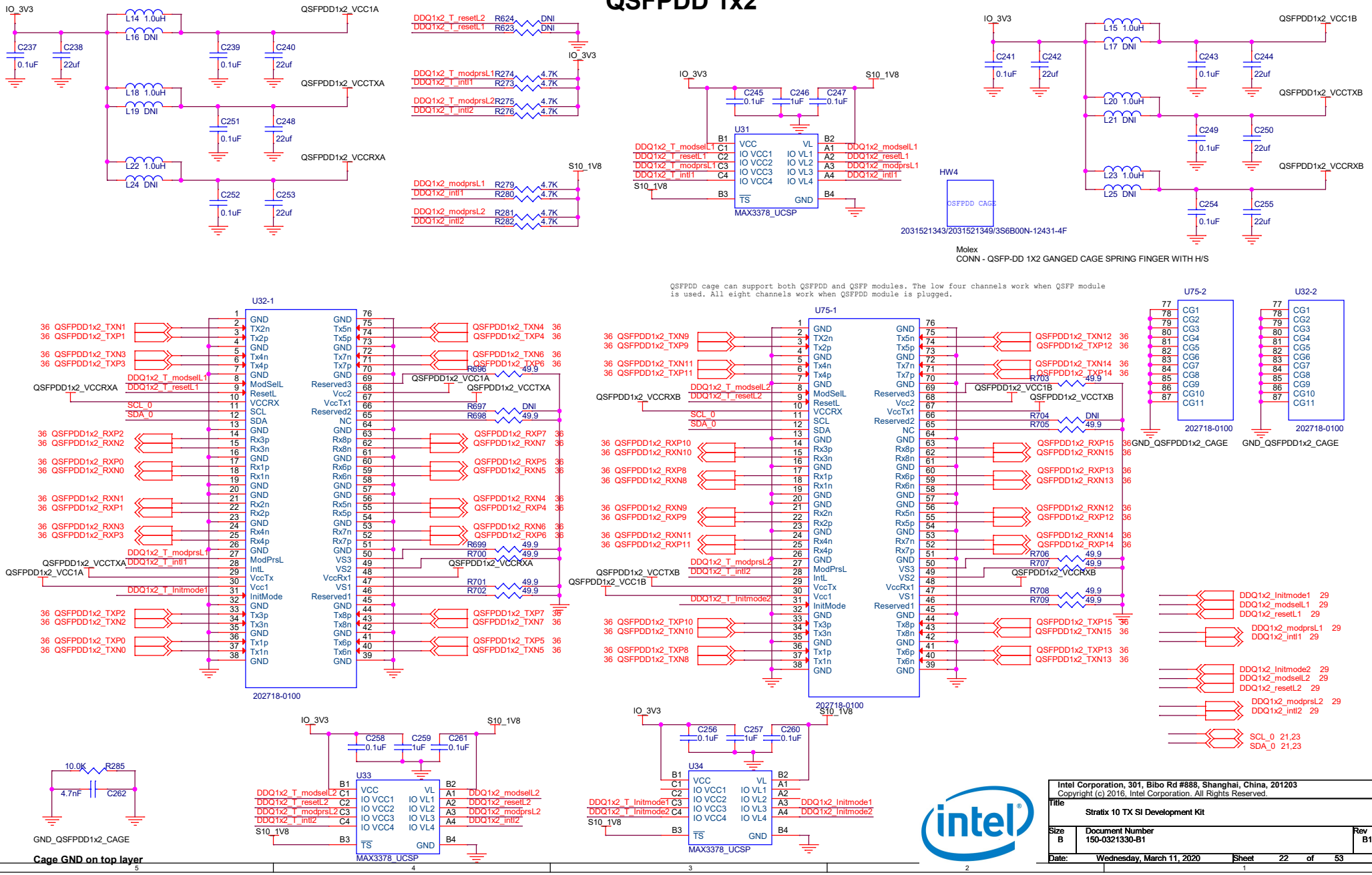
QSFPDD 1x2



QSFPDD cage can support both QSFPDD and QSFP modules. The low four channels work when QSFP module is used. All eight channels work when QSFPDD module is plugged.

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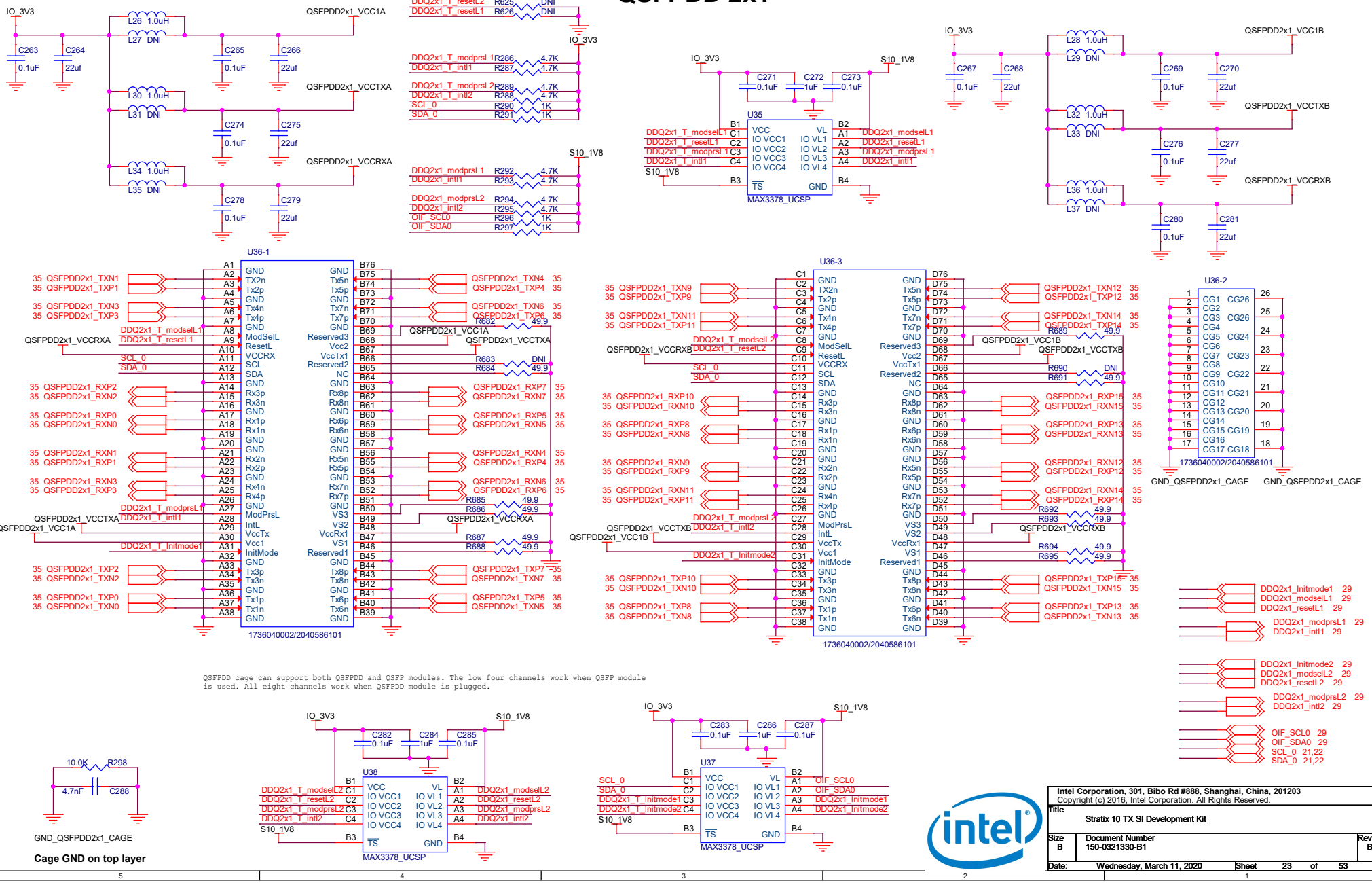
QSFPDD 2x1



QSFPDD cage can support both QSFPDD and QSFP modules. The low four channels work when QSFP module is used. All eight channels work when QSFPDD module is plugged.

Cage GND on top layer

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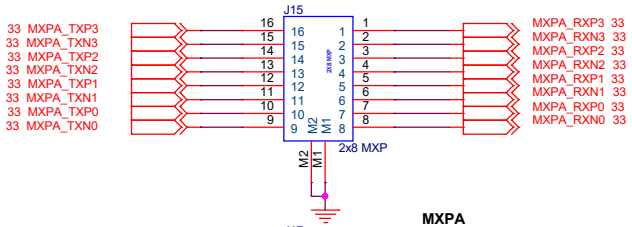
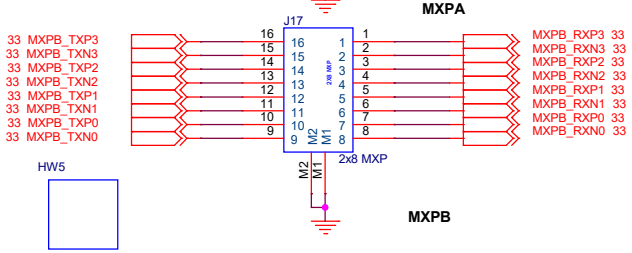
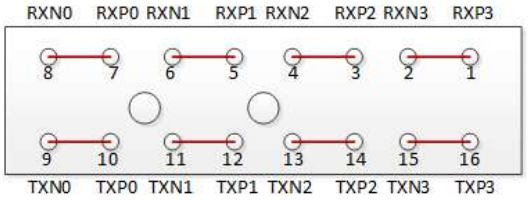
MXP / 2.4mm Connectors



MXPA



MXPB



HW5

73415-8230

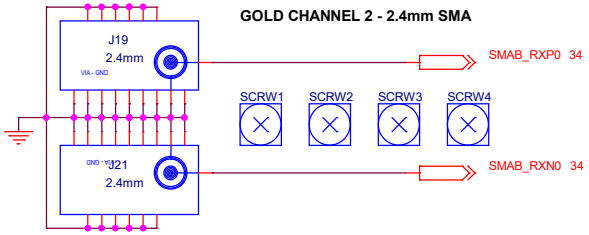
Molex
WASHER AND BACKPLATE FOR 2.4MM MOLEX RF CONNECTOR

HW9

73415-8230

Molex
WASHER AND BACKPLATE FOR 2.4MM MOLEX RF CONNECTOR

GOLD CHANNEL 2 - 2.4mm SMA



HW6

73415-8230

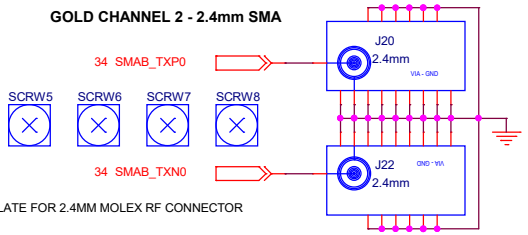
Molex
WASHER AND BACKPLATE FOR 2.4MM MOLEX RF CONNECTOR

HW7

73415-8230

Molex
WASHER AND BACKPLATE FOR 2.4MM MOLEX RF CONNECTOR

GOLD CHANNEL 2 - 2.4mm SMA



HW10

73415-8230

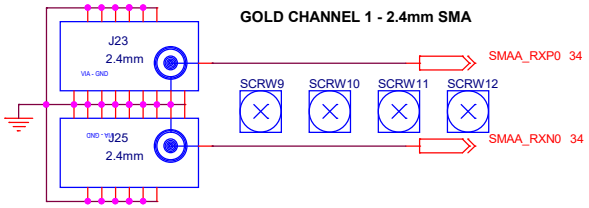
Molex
WASHER AND BACKPLATE FOR 2.4MM MOLEX RF CONNECTOR

HW11

73415-8230

Molex
WASHER AND BACKPLATE FOR 2.4MM MOLEX RF CONNECTOR

GOLD CHANNEL 1 - 2.4mm SMA

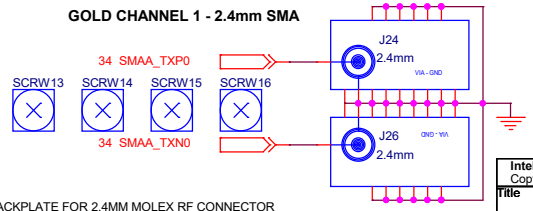


HW8

73415-8230

Molex
WASHER AND BACKPLATE FOR 2.4MM MOLEX RF CONNECTOR

GOLD CHANNEL 1 - 2.4mm SMA



HW12

73415-8230

Molex
WASHER AND BACKPLATE FOR 2.4MM MOLEX RF CONNECTOR

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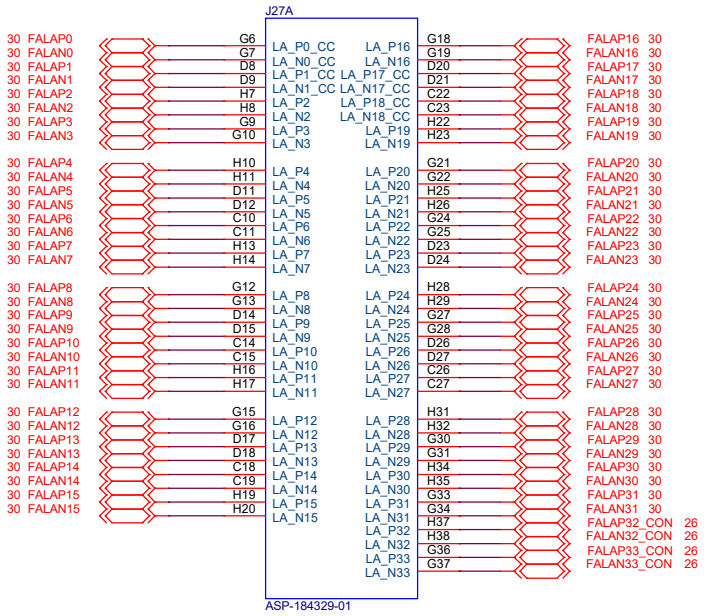
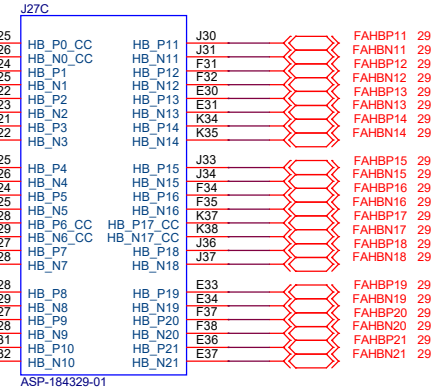
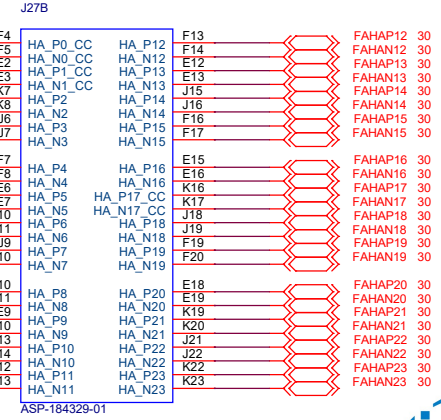
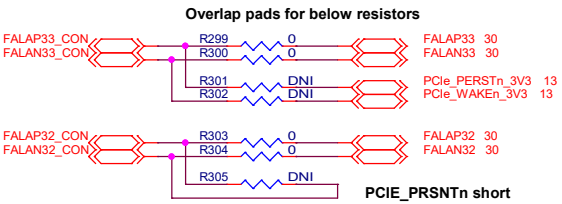
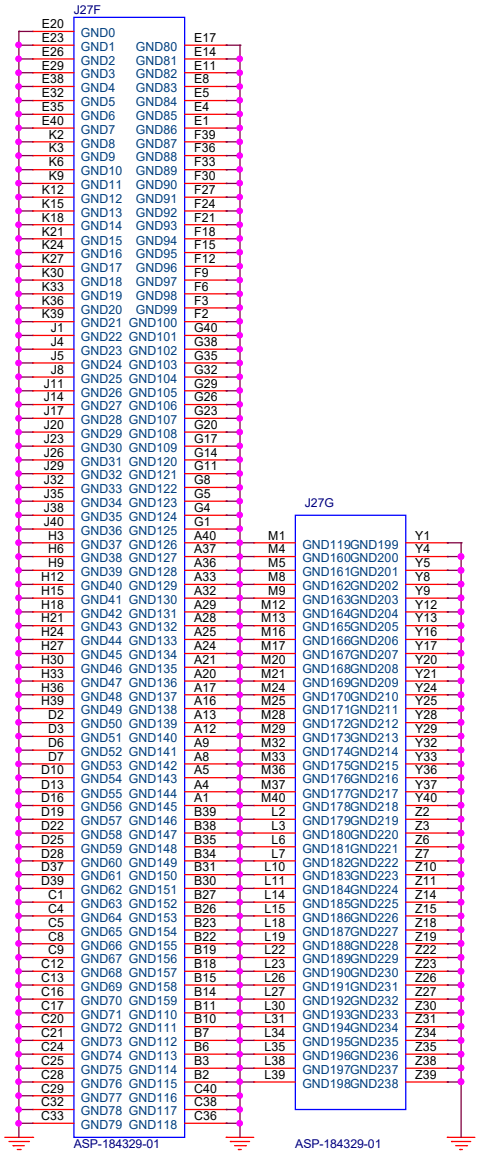
FMC+ 1











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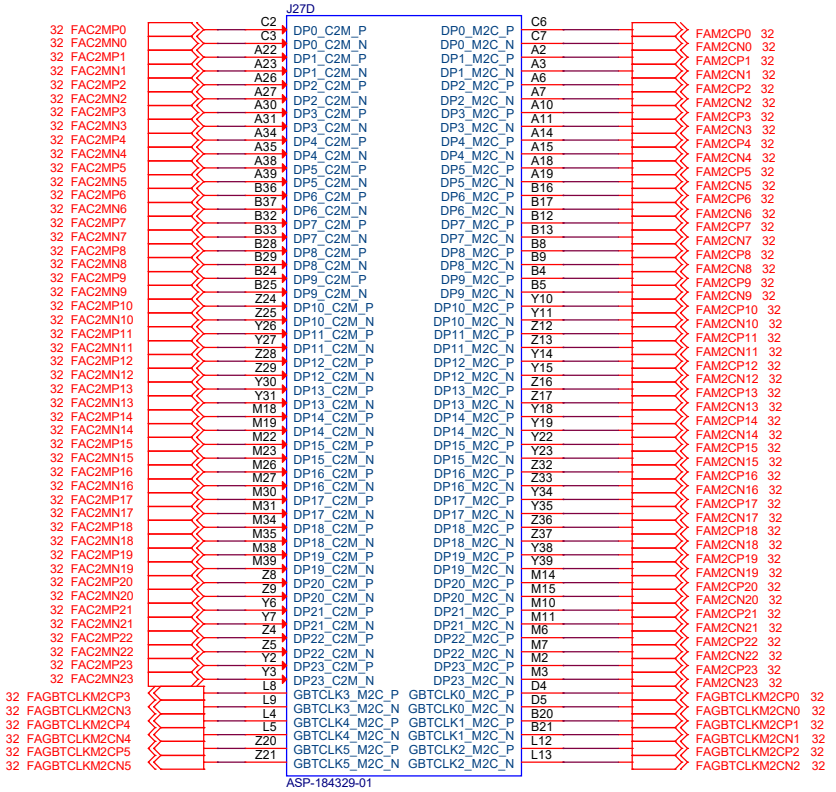
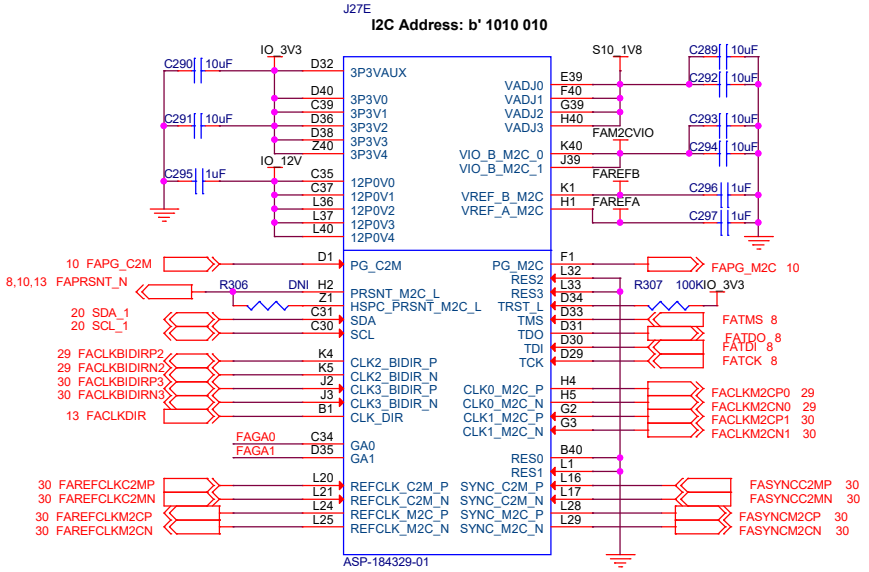
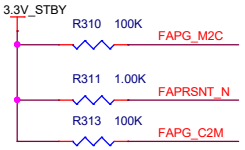
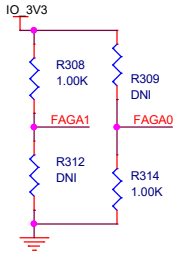
FMC+ 2





PCIE REFCLK





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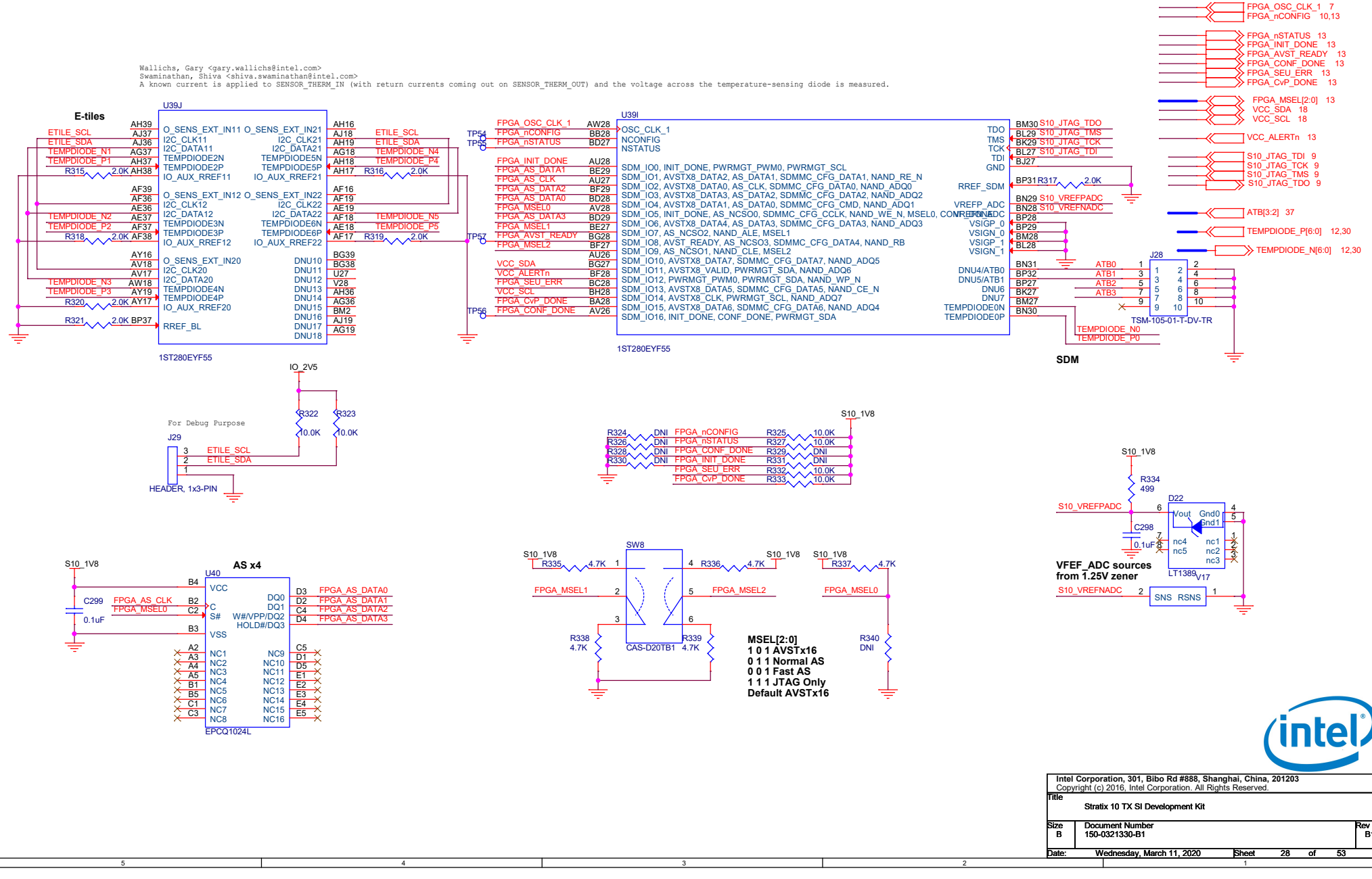
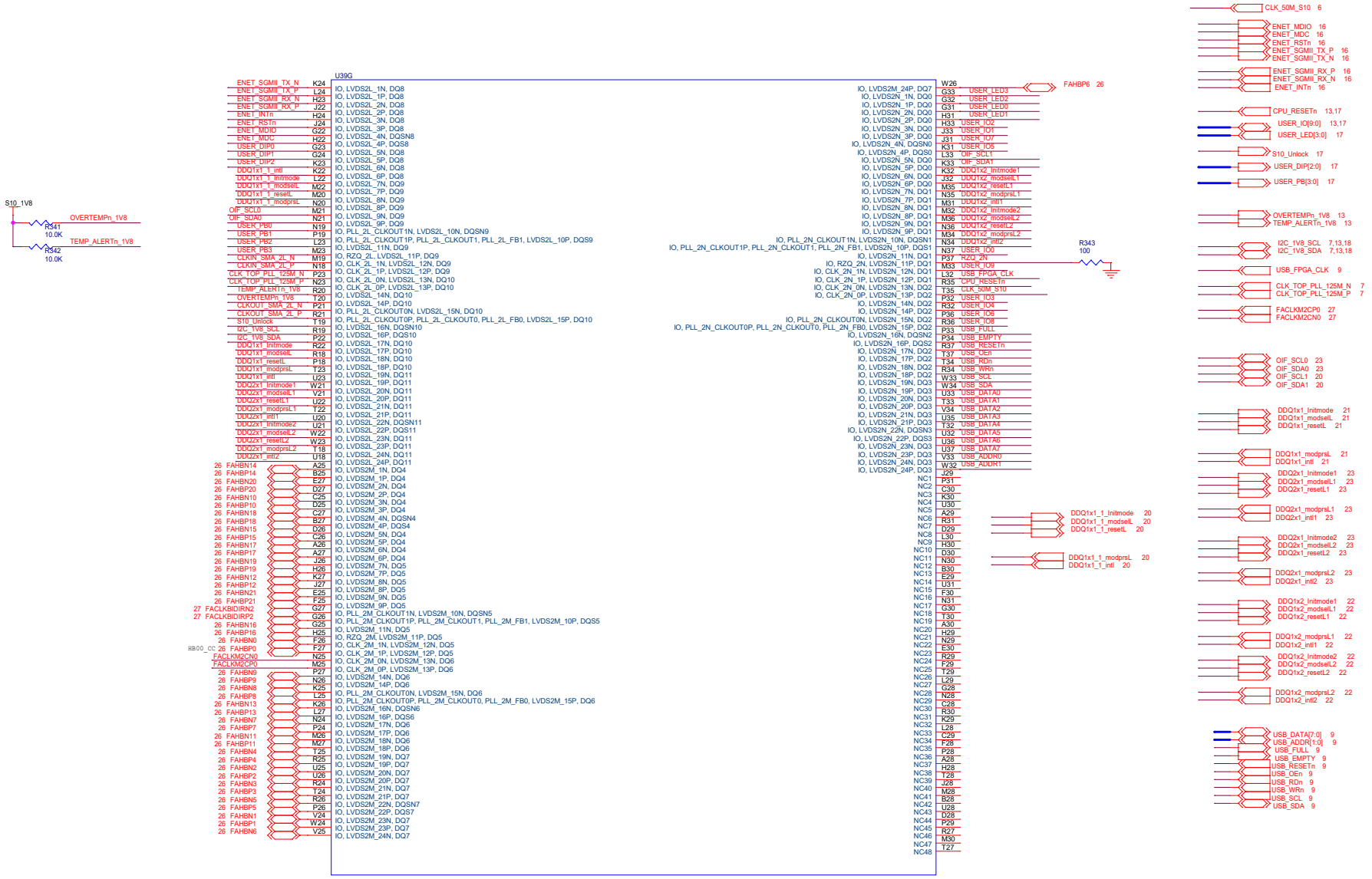
S10 Banks - SDM



S10 Top Banks 2 L/M/N



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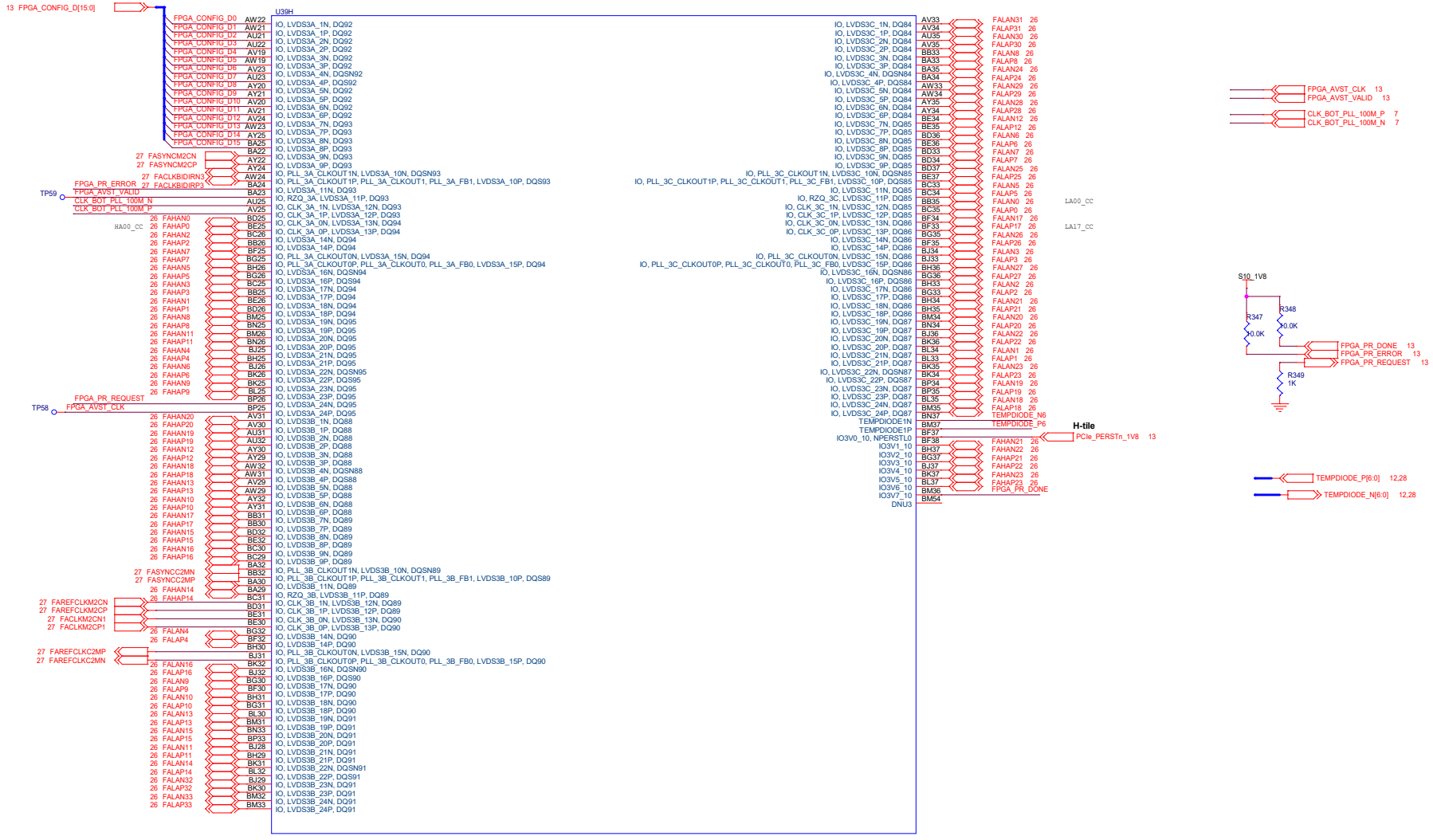
S10 Bottom Banks - 3A/B/C



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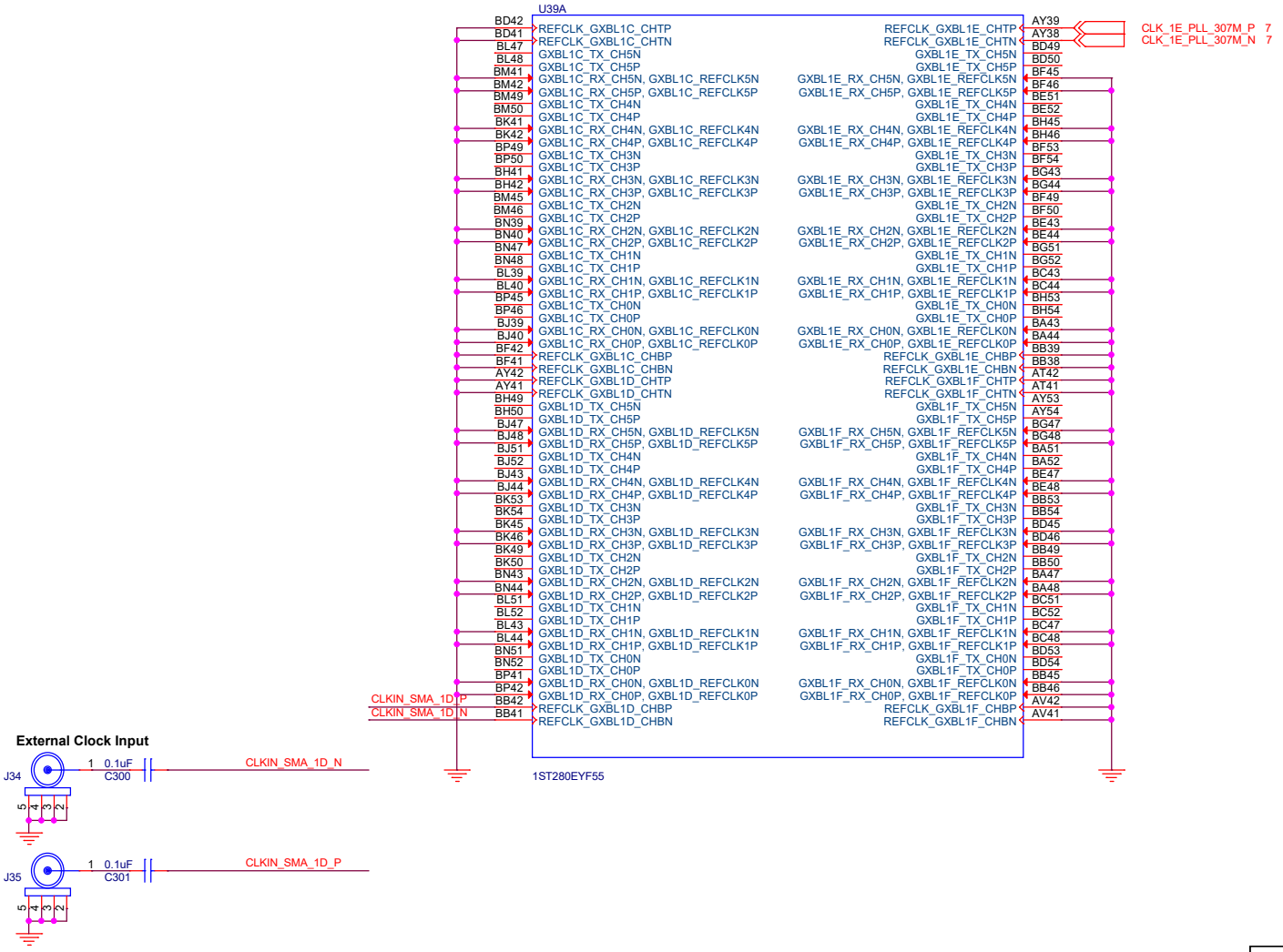
S10 HTile Banks - 1C/D/E/F



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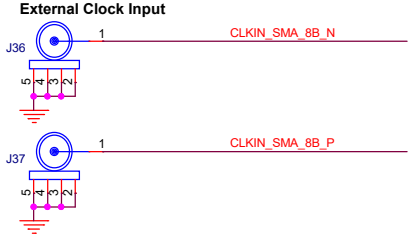
S10 ETile Banks - 8B

External Clock Input



Check the latest PCG for the connection of unused pins in the E-tiles

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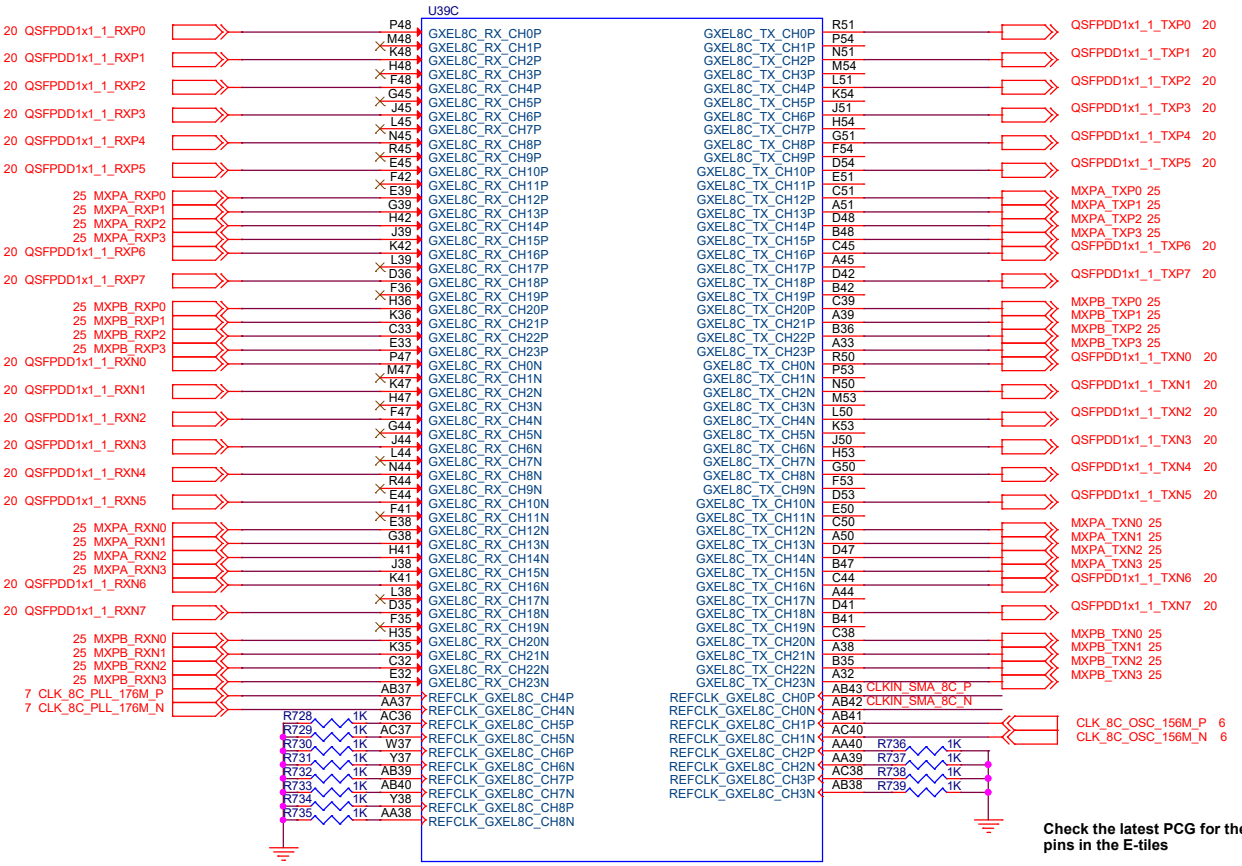
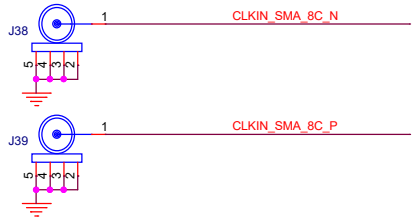
S10 ETile Banks - 8C

QSFPDD1x1 Port:
100G with PAM4
Channel 1: 0/2; Channel 2: 8/10
Channel 3: 4/6; Channel 4: 16/18
200G with PAM4
Channel 1: 0/2/4/6
Channel 2: 8/10/16/18
400G with PAM4
Channel 0/2/4/6/8/10/16/18



Check the latest PCG for the connection of unused pins in the E-tiles

External Clock Input



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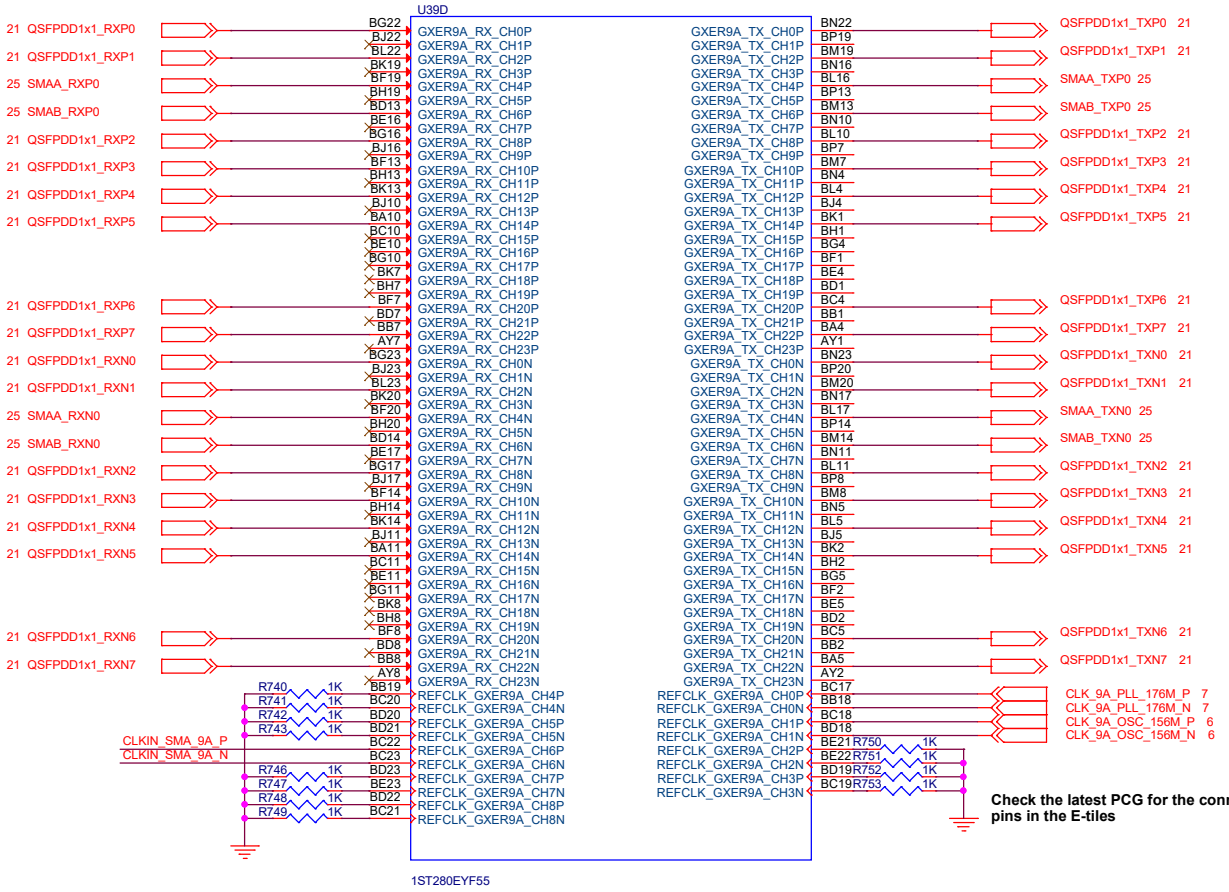
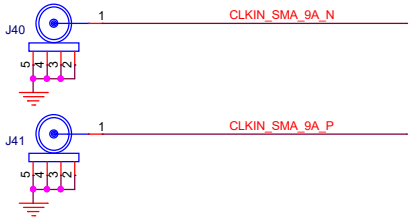
S10 ETile Banks - 9A

QSFPDD1x1 Port:
100G with PAM4
Channel 1: 0/2; Channel 2: 8/10
Channel 3: 12/14; Channel 4: 20/22
200G with PAM4
Channel 1: 0/2/8/10
Channel 2: 12/14/20/22
400G with PAM4
Channel 0/2/8/10/12/14/20/22



Check the latest PCG for the connection of unused pins in the E-tiles

External Clock Input



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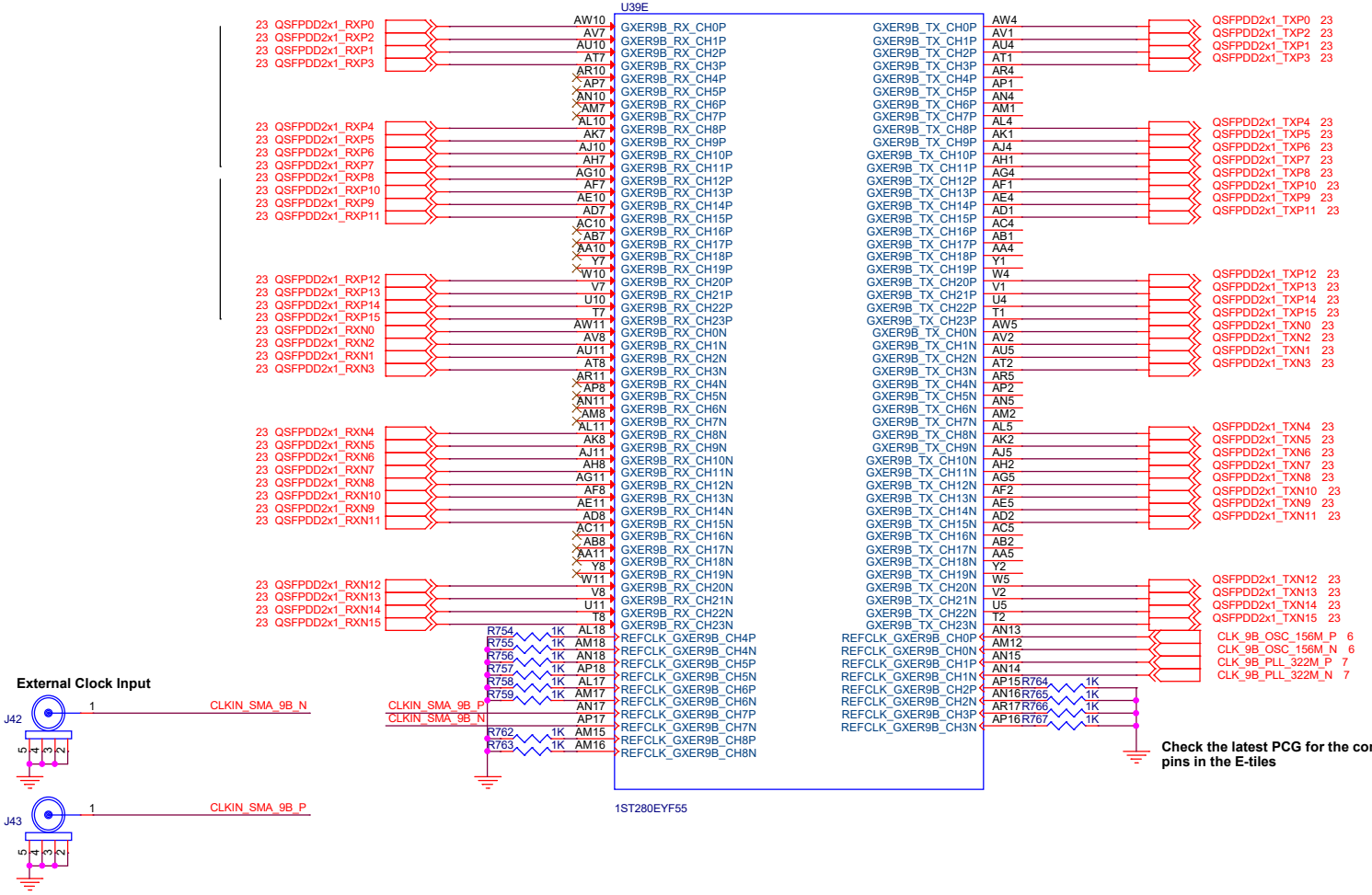
S10 ETile Banks - 9B

QSFPDD2x1 Port 1:
100G with 28G NRZ
Channel 1: 0/1/2/3
Channel 2: 8/9/10/11
100G with PAM4
Channel: 0/2

QSFPDD2x1 Port 2:
100G with 28G NRZ
Channel 1: 12/13/14/15
Channel 2: 20/21/22/23
100G with PAM4
Channel: 12/14



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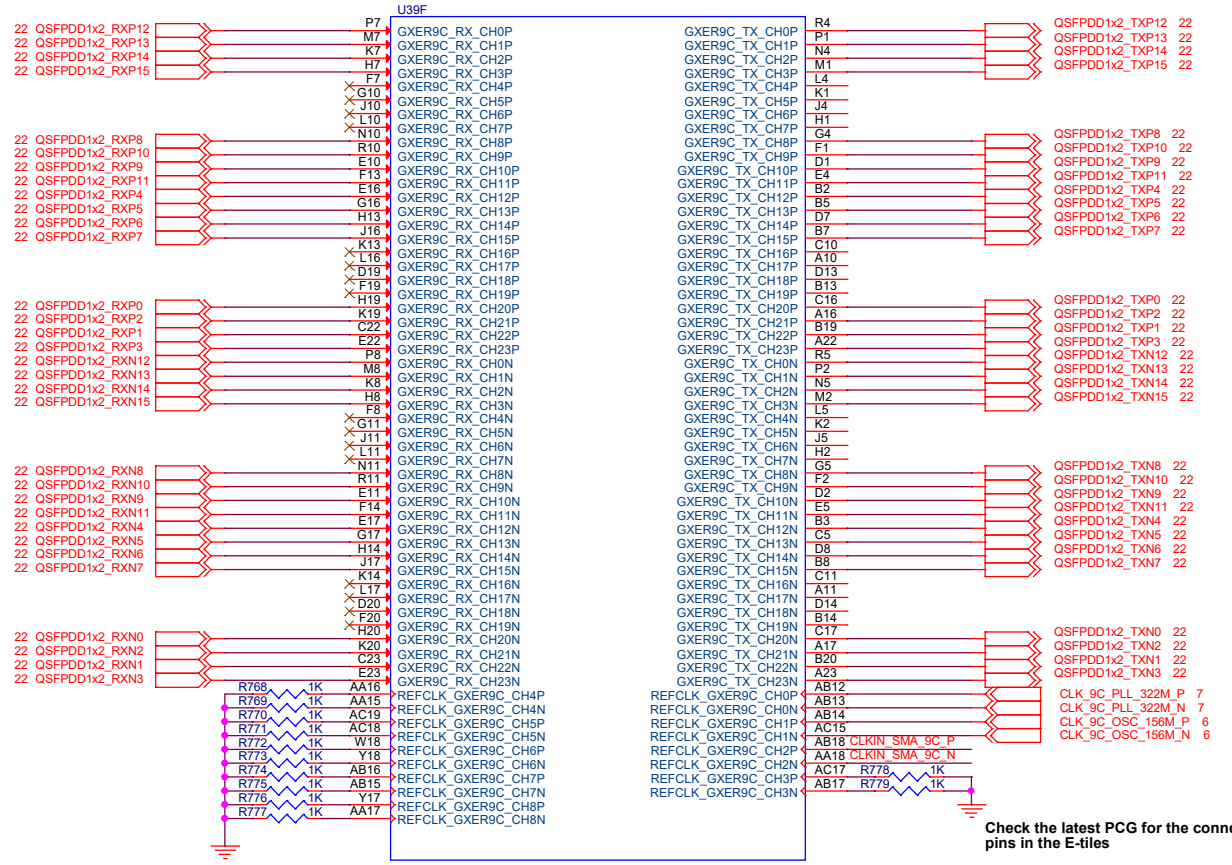
S10 ETile Banks - 9C

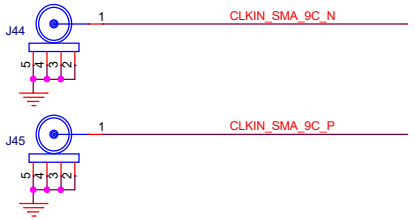
QSFPDD1x2Port 1:
100G with 28G NRZ
Channel 1: 0/1/2/3
Channel 2: 8/9/10/11
100G with PAM4
Channel: 8/9

QSFPDD1x2 Port 2:
100G with 28G NRZ
Channel 1: 12/13/14/15
Channel 2: 20/21/22/23
100G with PAM4
Channel: 20/22



Check the latest PCG for the connection of unused pins in the E-tiles

External Clock Input



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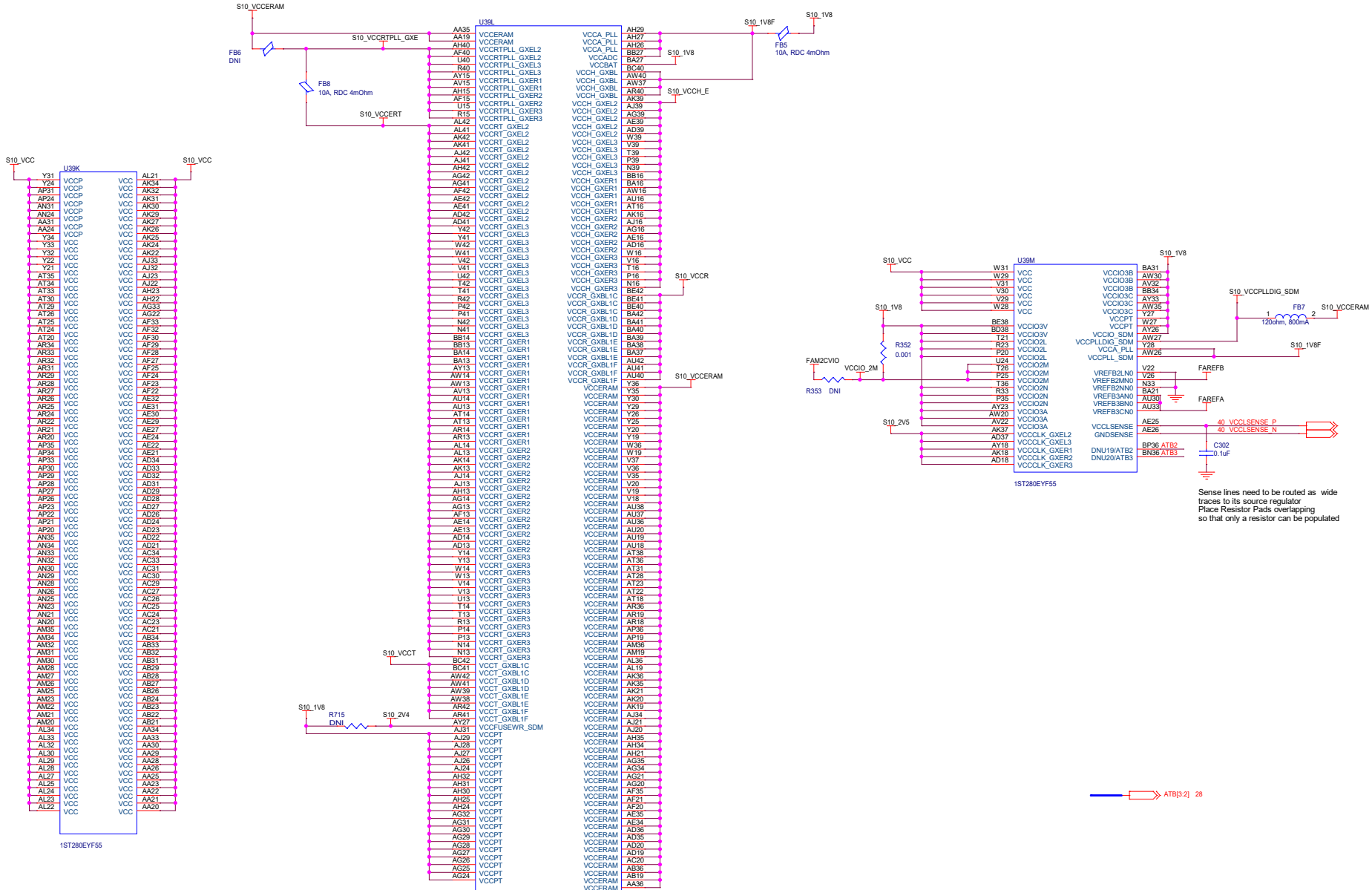
S10 PWR



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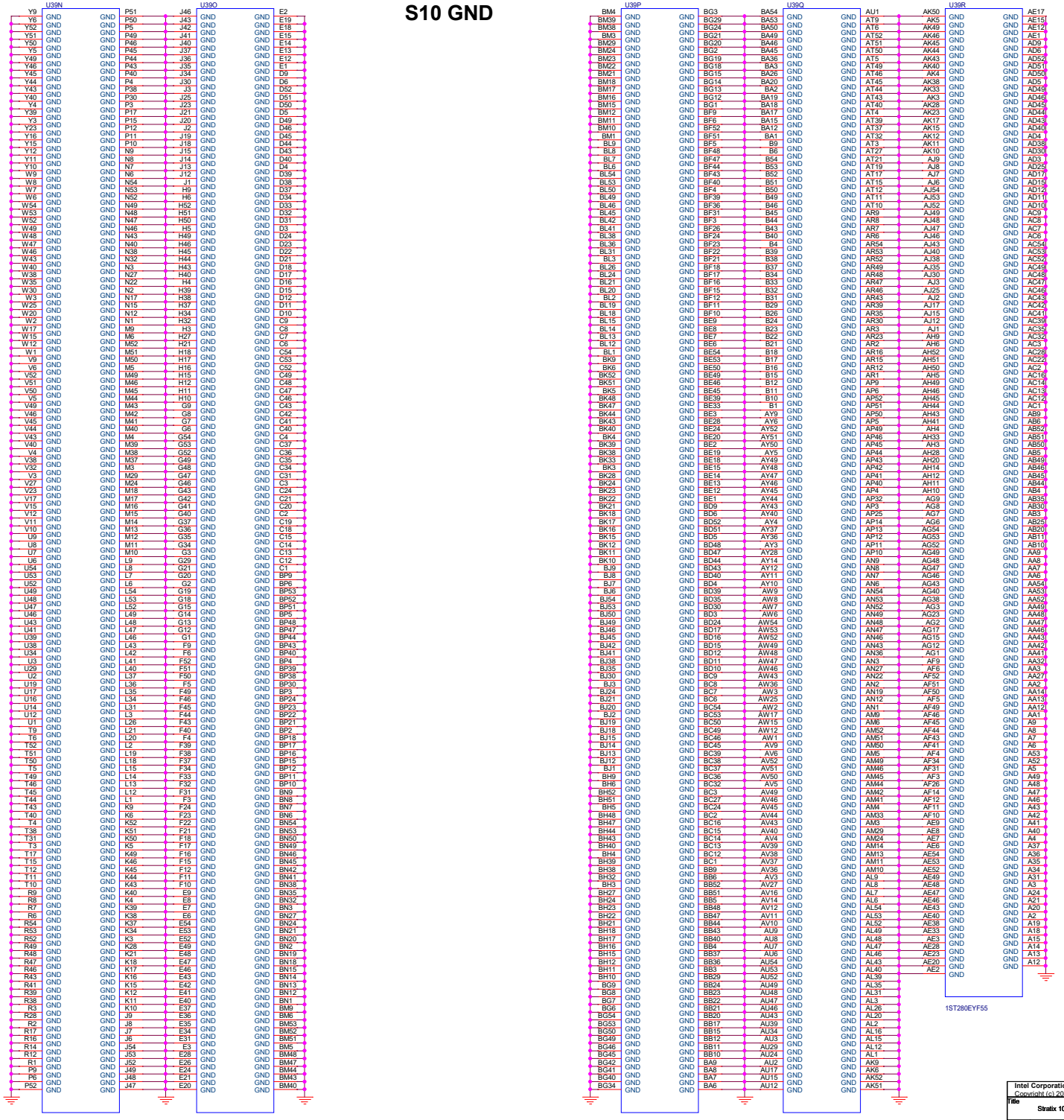
S10 GND



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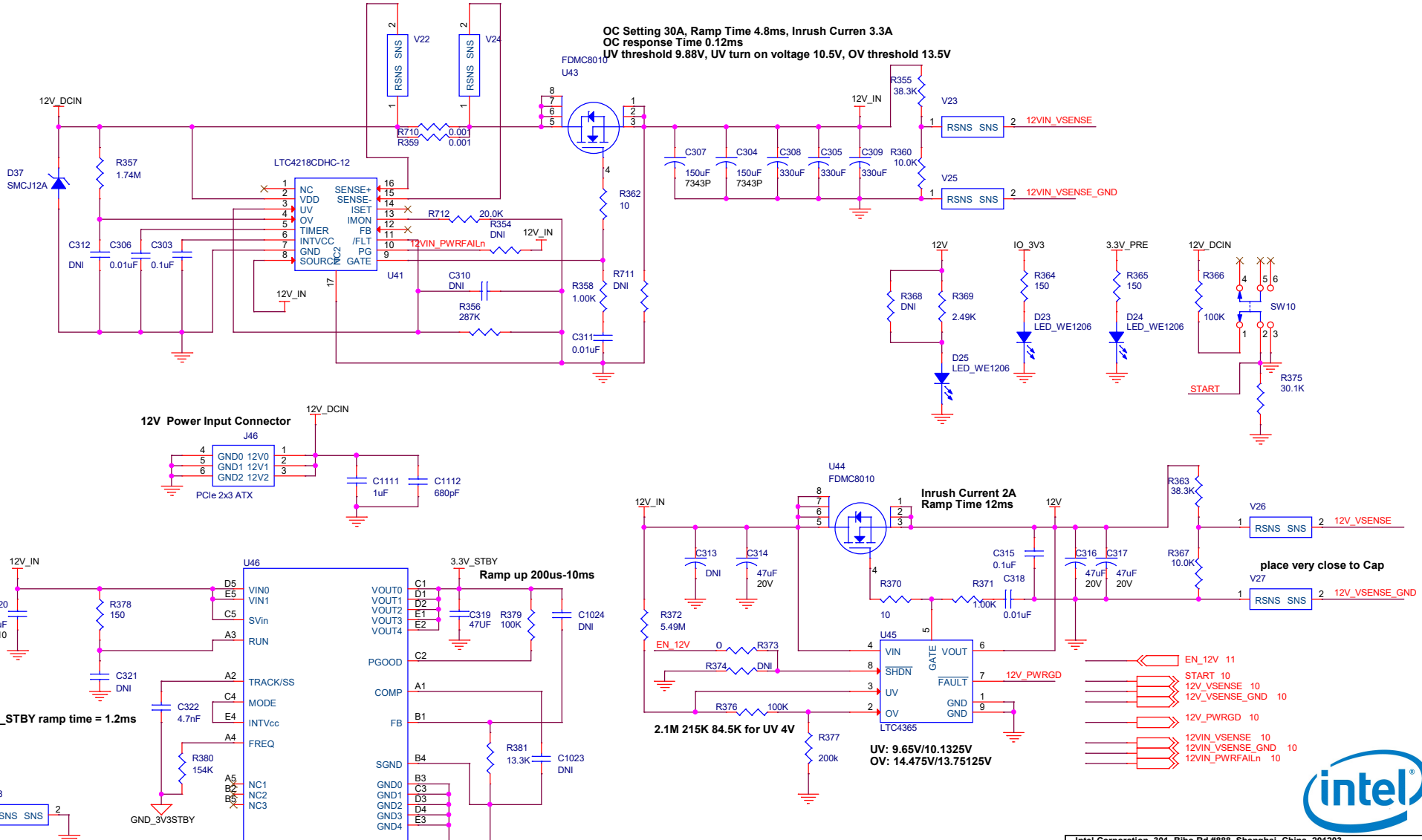
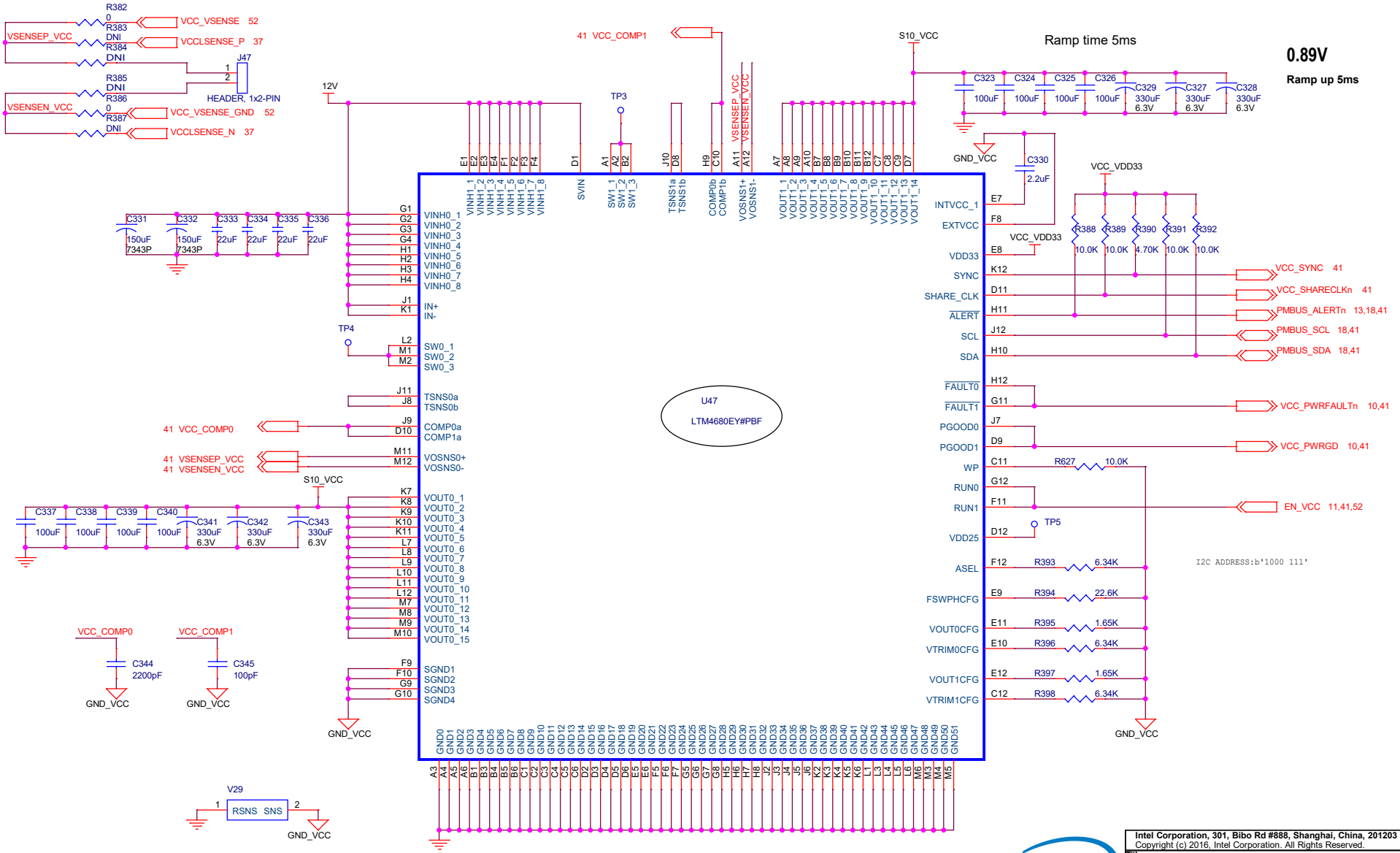
PWR - POWER INPUT



PWR - VCC 1



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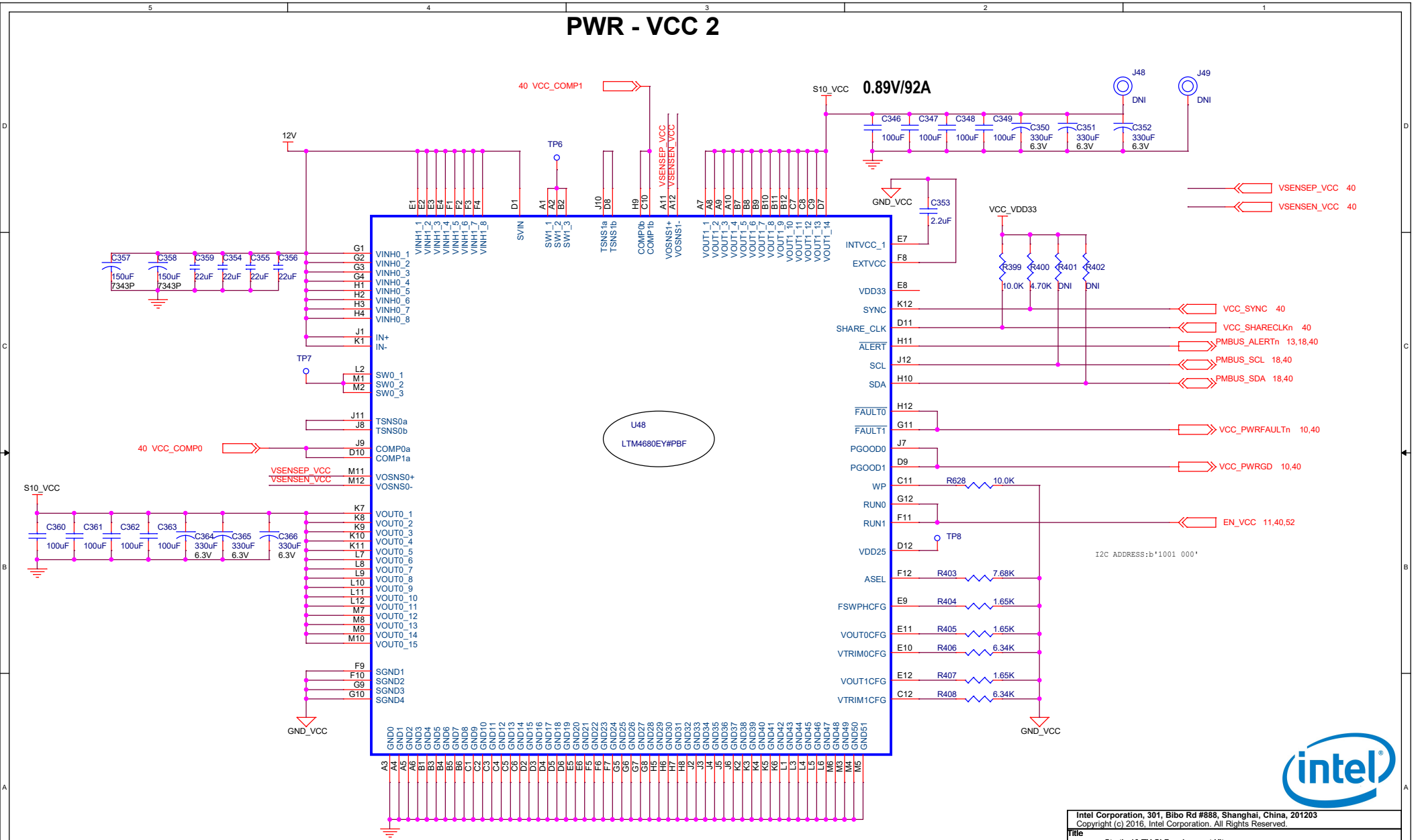
PWR - VCC 2



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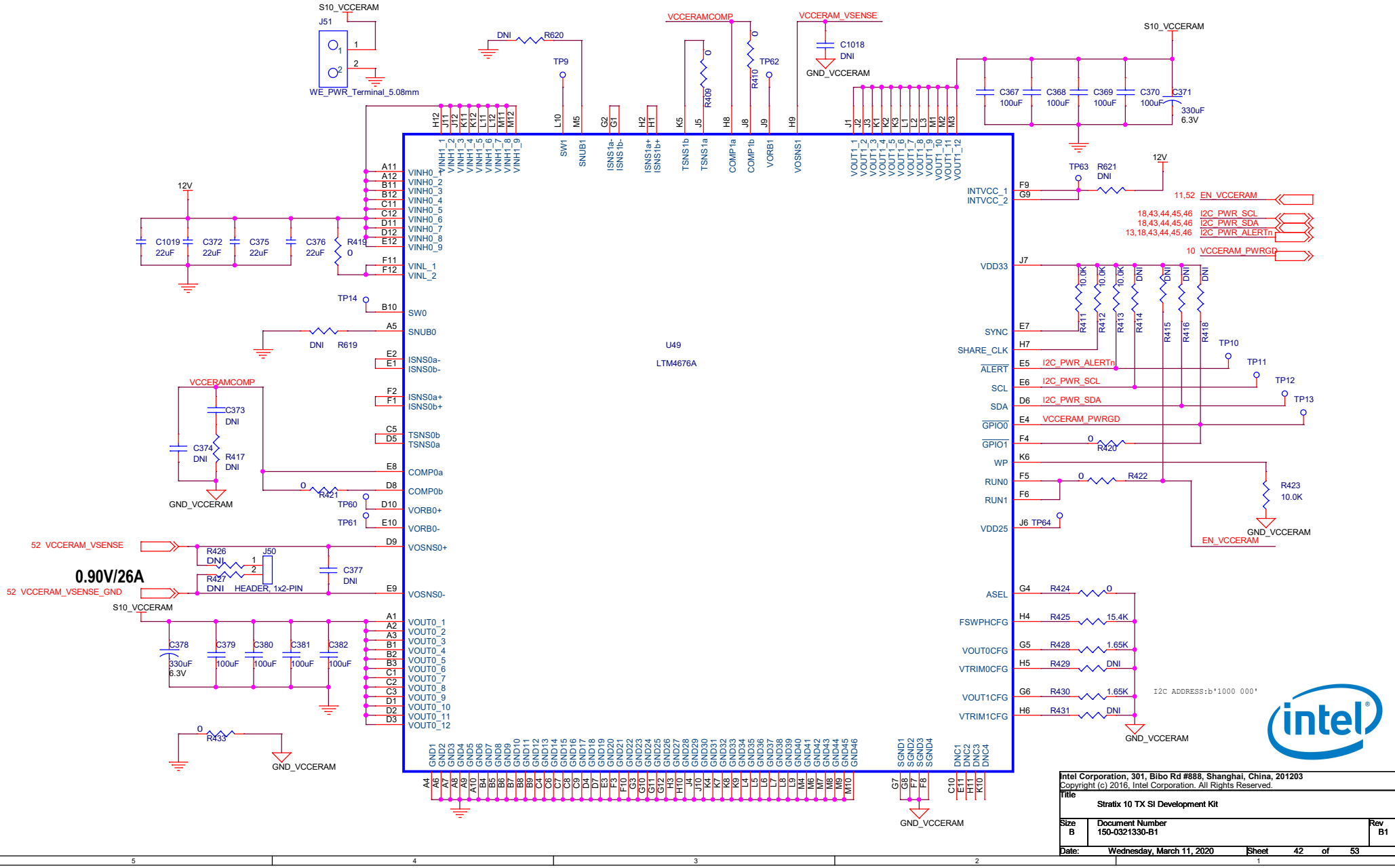
PWR - VCCERAM



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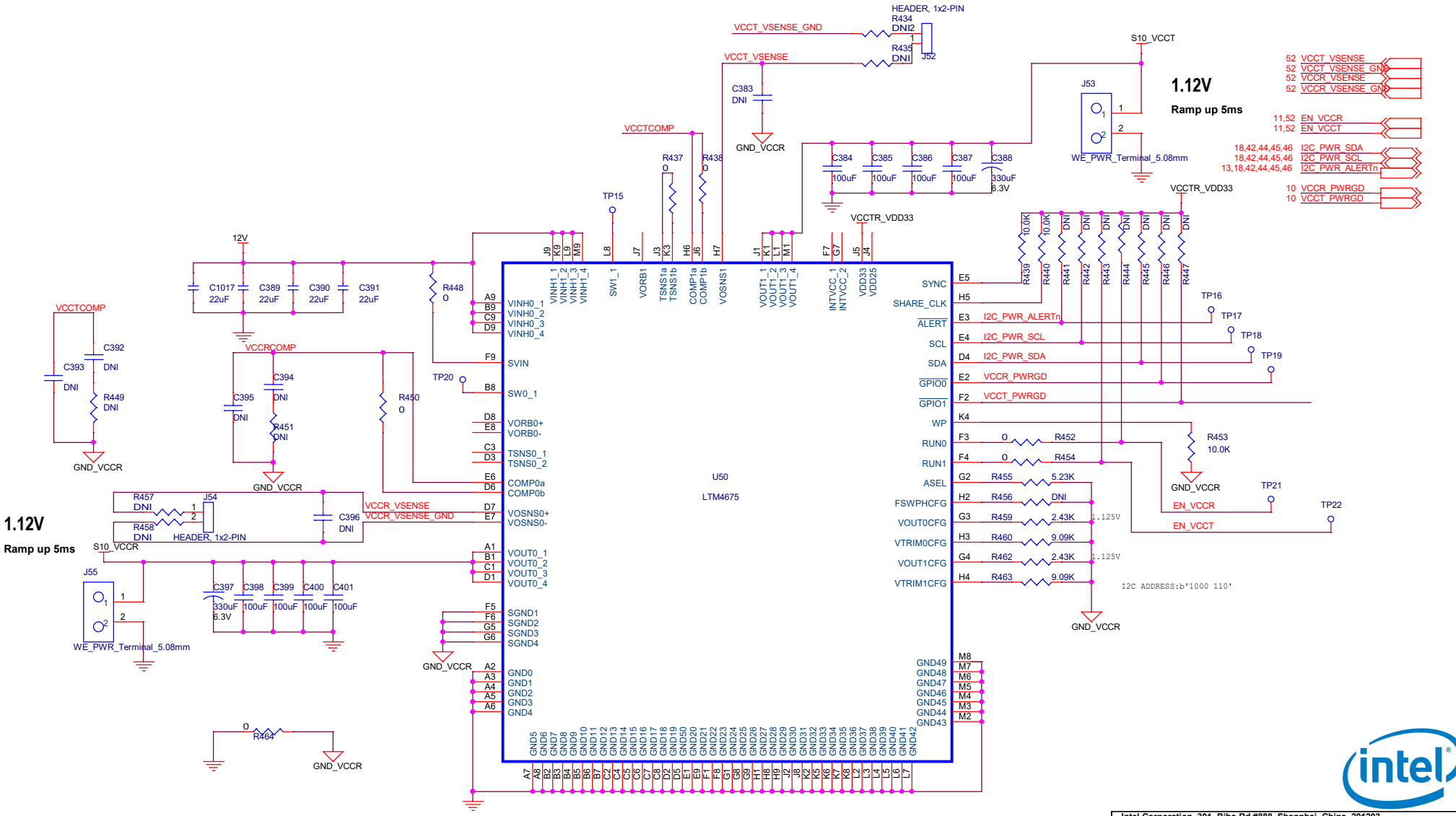
PWR VCCT/VCCR



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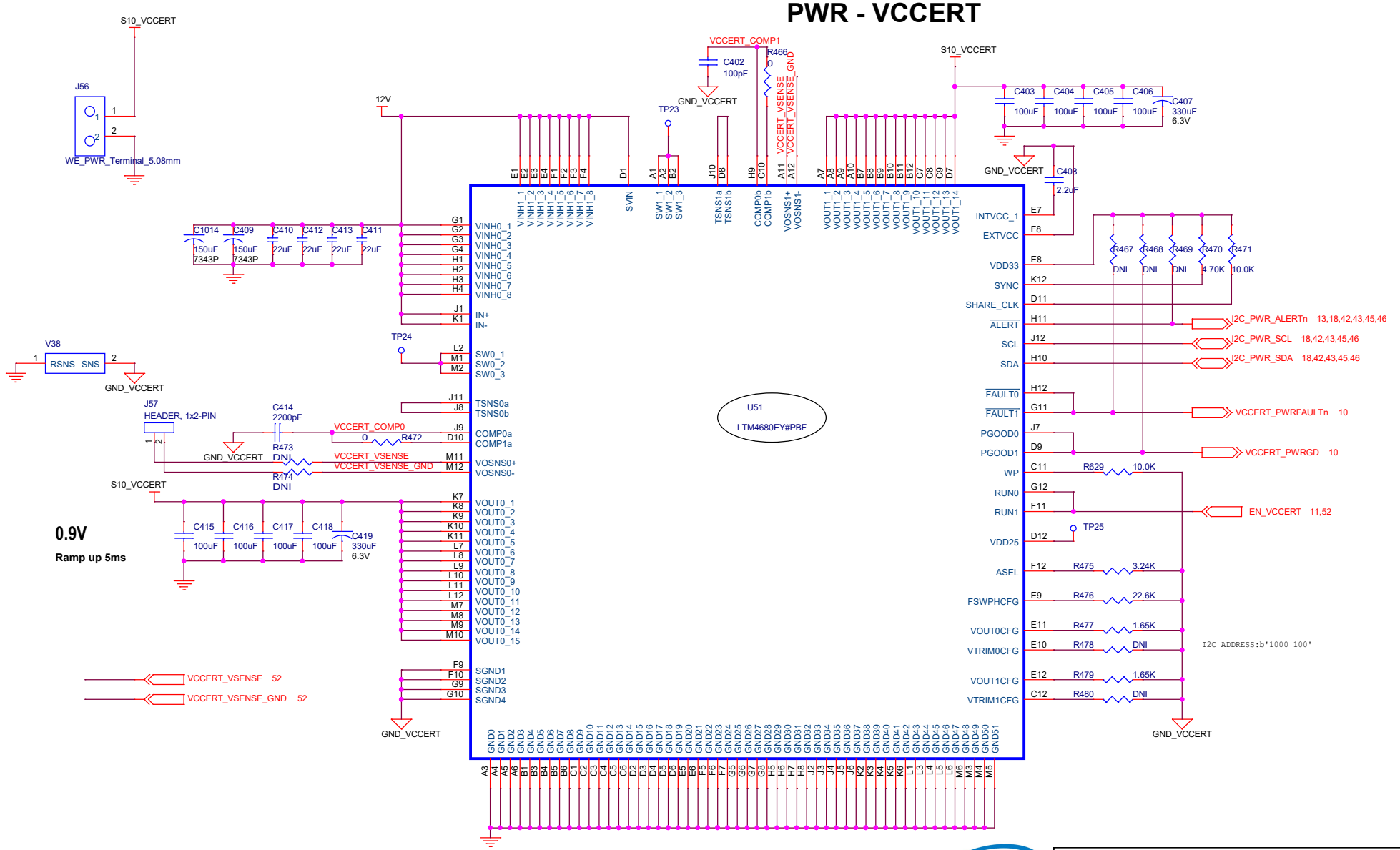
PWR - VCCERT



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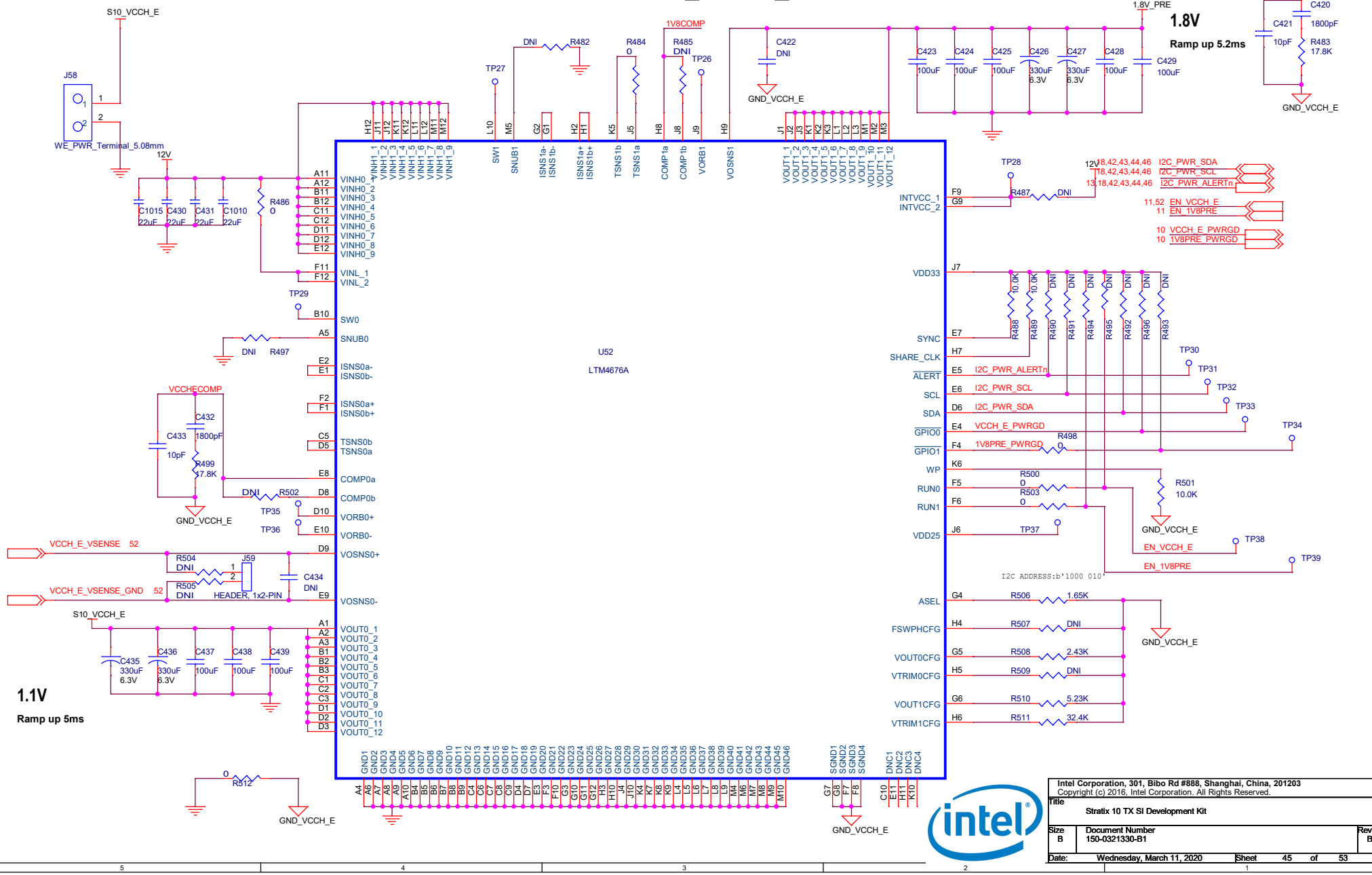
PWR - VCCH_E/1.8V_PRE



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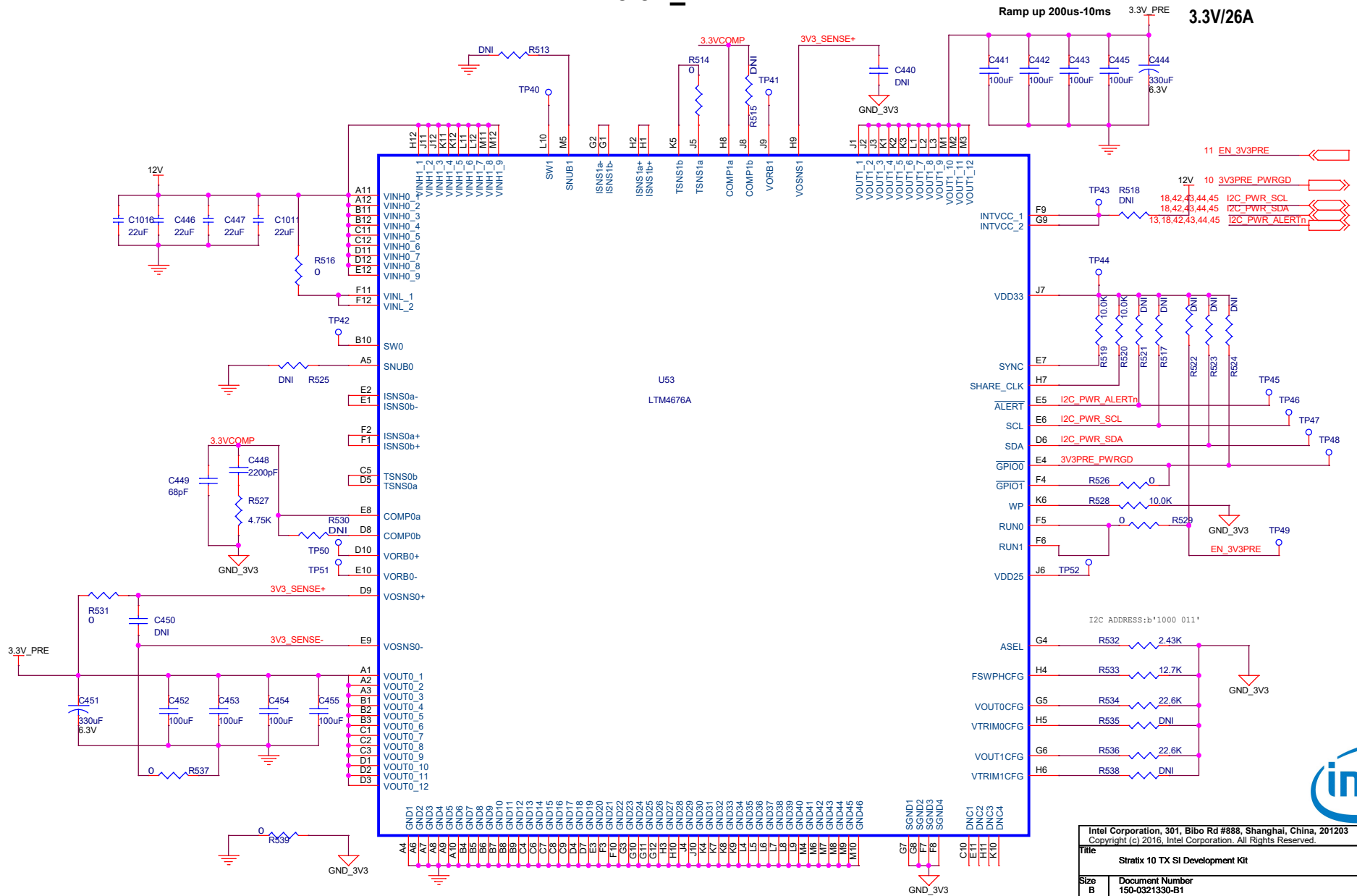
PWR - 3.3V_PRE


Ramp up 200us-10ms
3.3V_PRE
3.3V/26A
U53
LTM4676A
3.3VCOMP
3V3_SENSE+
3V3_SENSE-
I2C ADDRESS:b'1000 011'
11 EN_3V3PRE
10 3V3PRE_PWRGD
18,42,43,44,45 I2C_PWR_SCL
18,42,43,44,45 I2C_PWR_SDA
13,18,42,43,44,45 I2C_PWR_ALERTn
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NA

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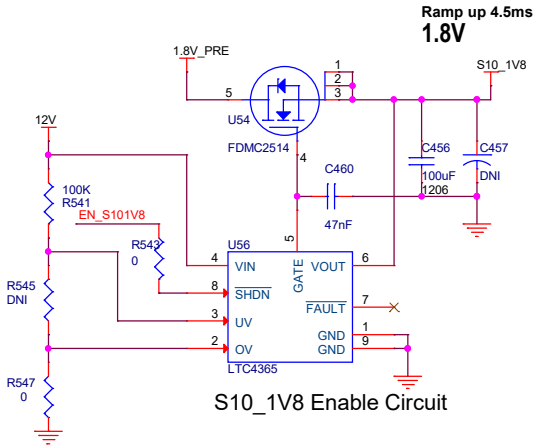
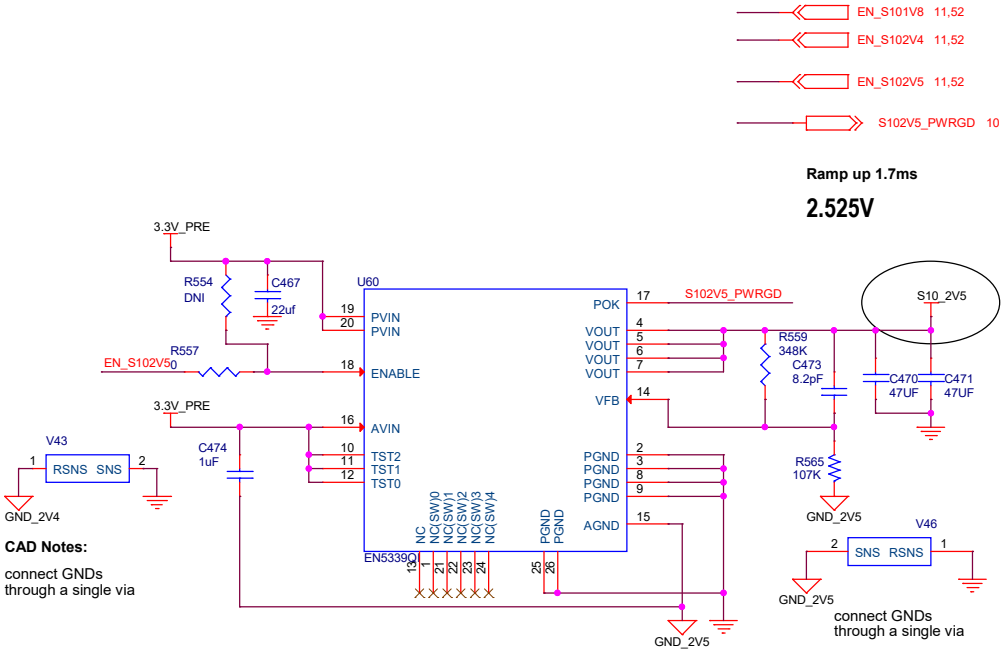
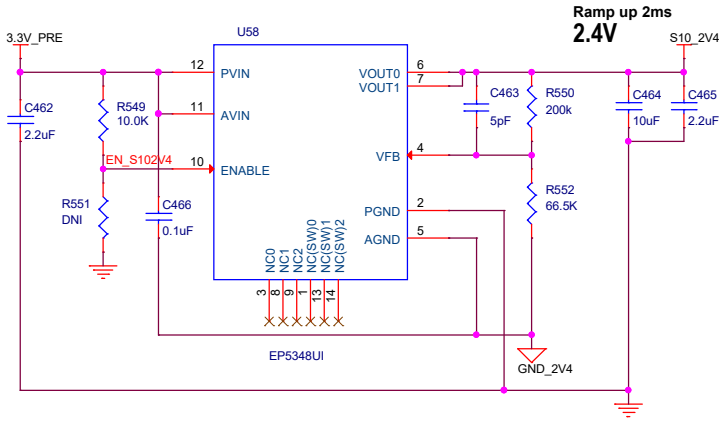
PWR - S10_1V8 S10_2V5 S10_2V4



S10_1V8 Enable Circuit





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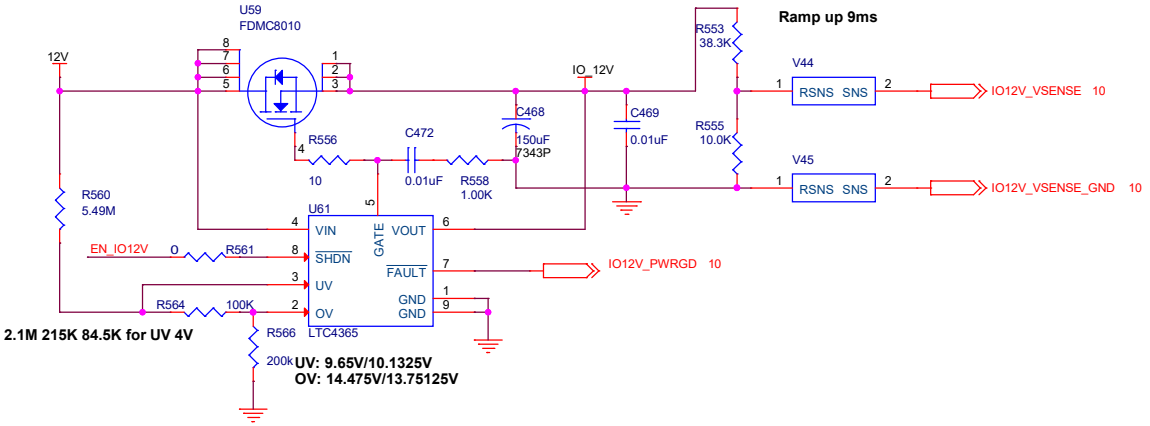
PWR - IO_2V5 IO_3V3 IO_12V

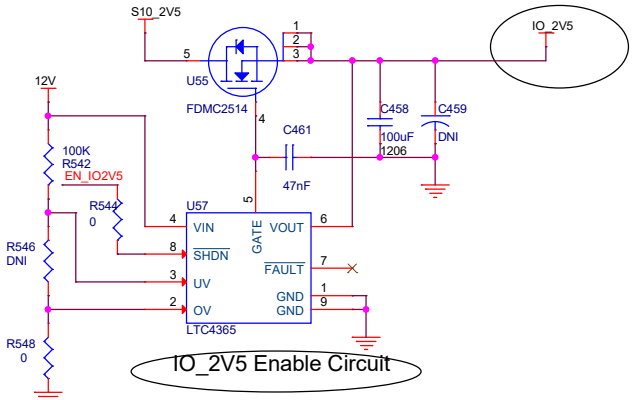
12V

Ramp up 9ms



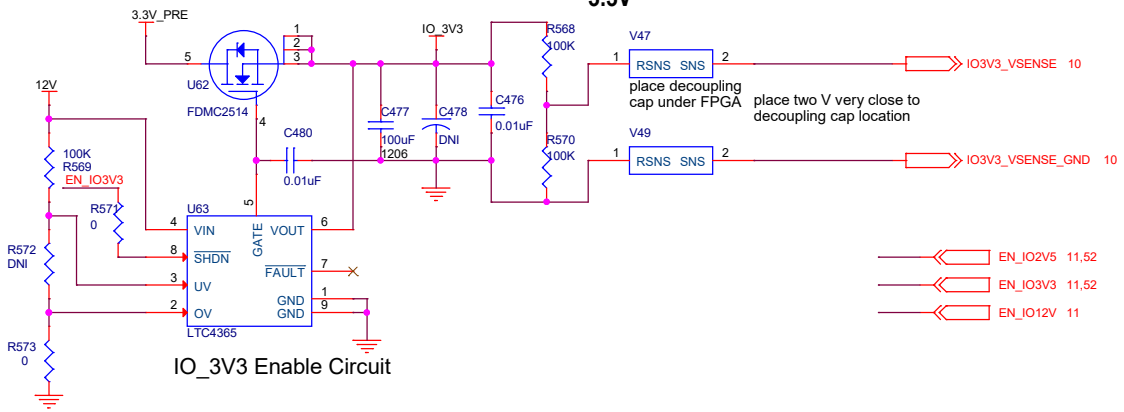
2.5V

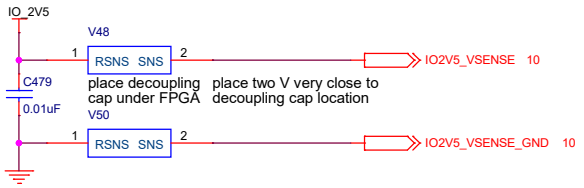
Ramp up 5.2ms



Ramp up 2.5ms

3.3V





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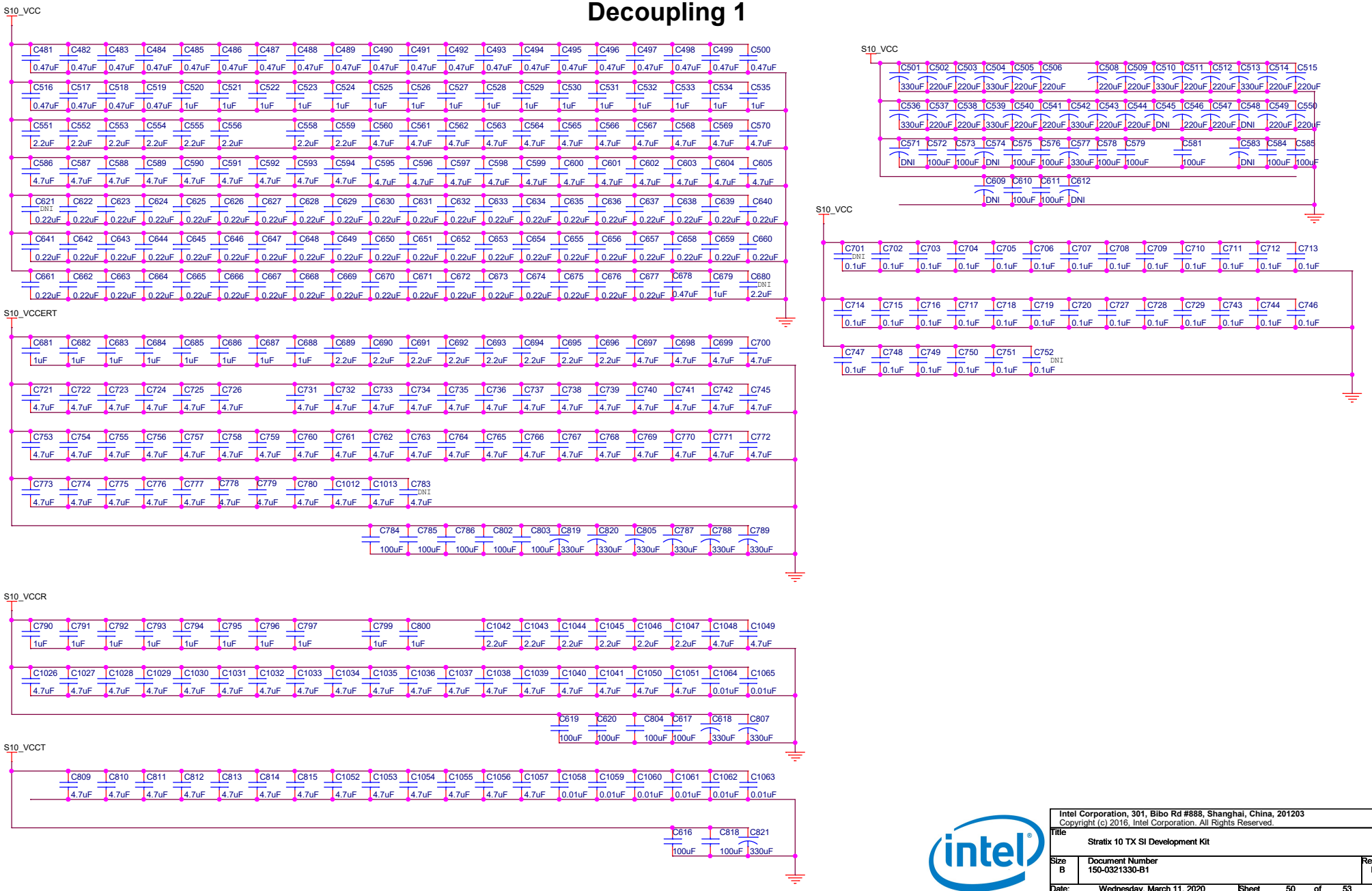
Decoupling 1



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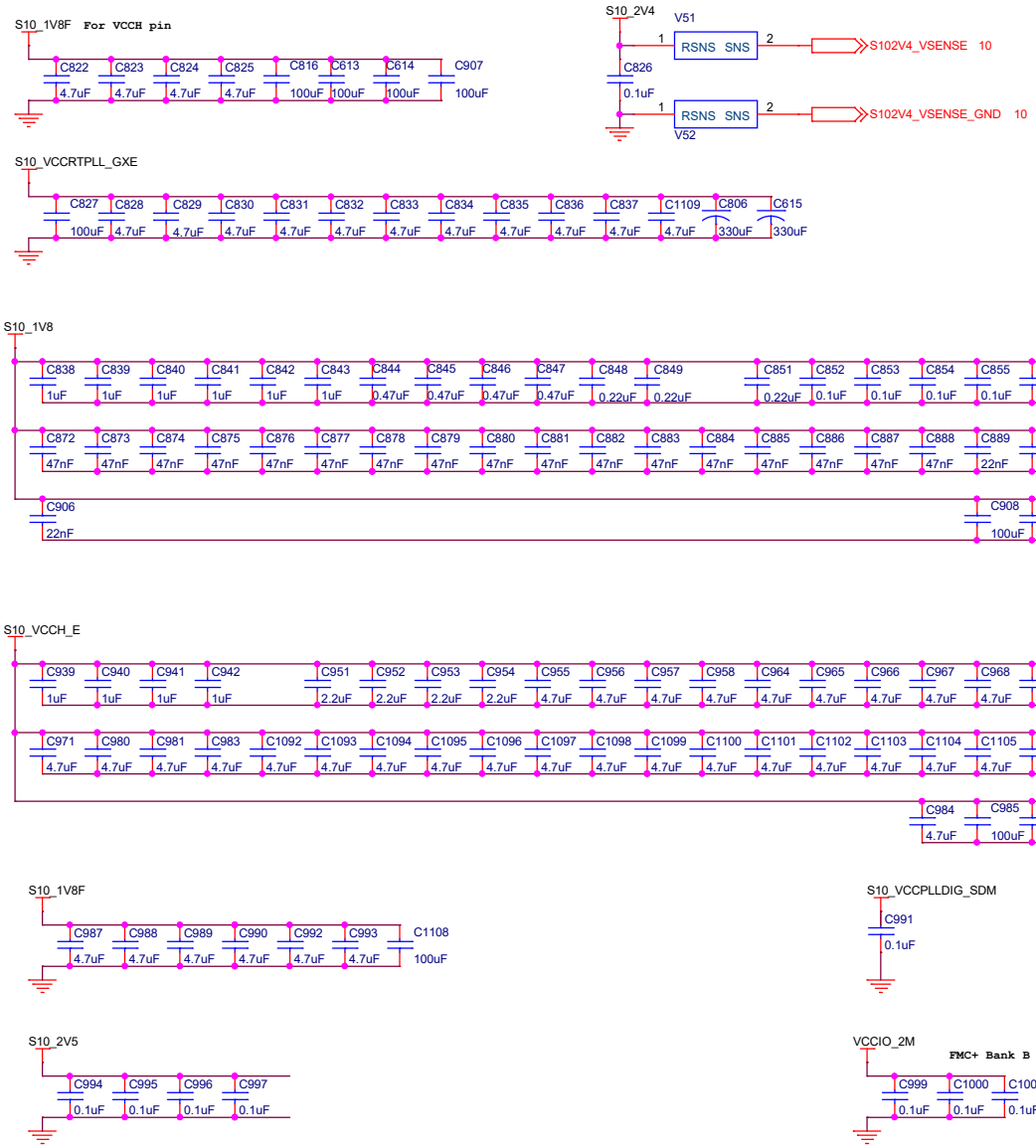
Decoupling 2



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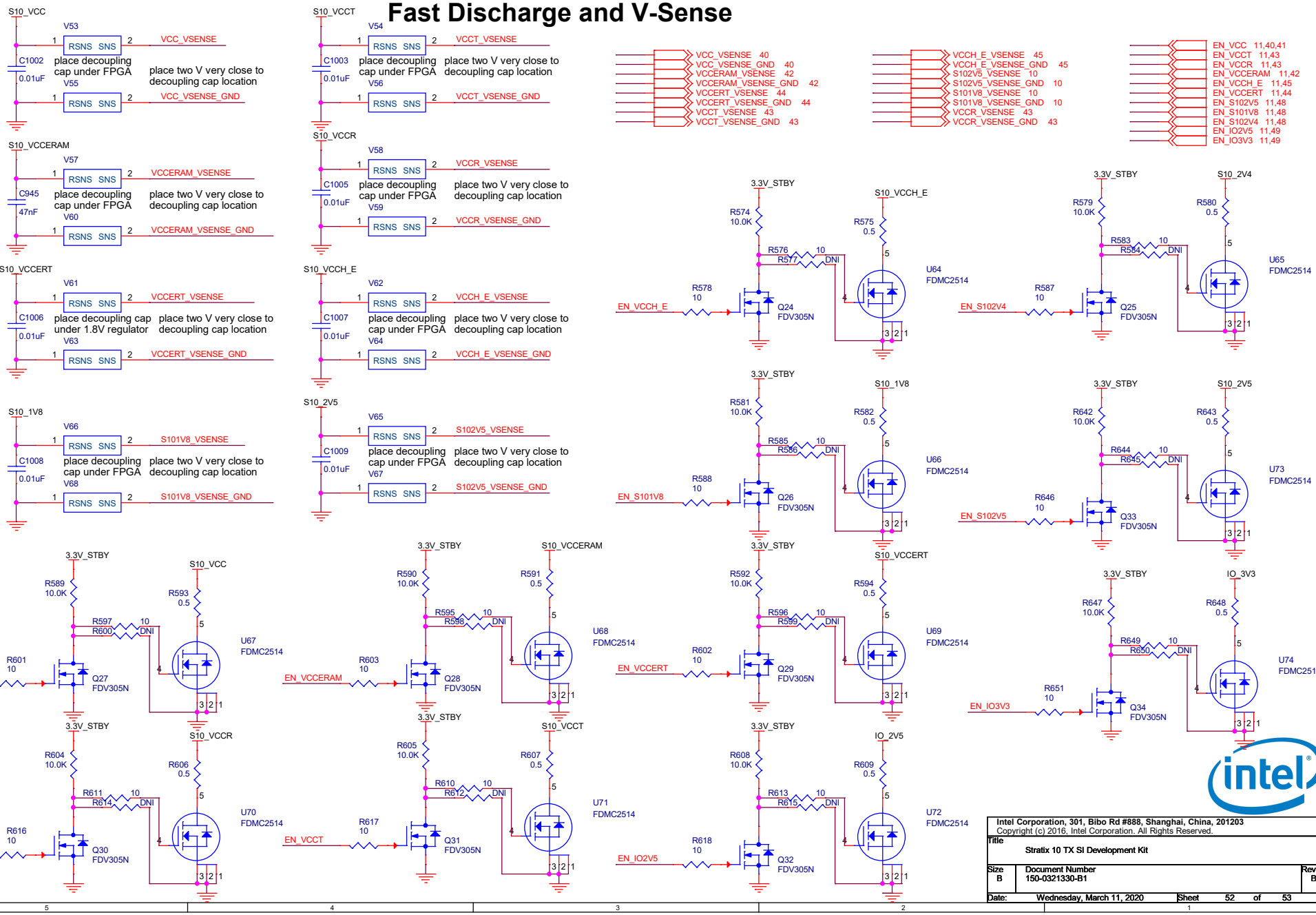
Fast Discharge and V-Sense



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Revision History

Ver.	DATE	PAGES	DESCRIPTION
B1			Change U22 VCCB to VCC_VDD33
B1			Unused E-tile reference clock pins are tied to GND with resistors, leave unused RX pin floating
B1			Replace OSFP and MXP with QSFPDD1x2 on left side
B1			Replace QSFPDD1x2 with FMC on right side
B1			Remove transceiver connection between FMC and H-tile
B1			Replace U47/U48/U51 with LTM4680EY#PBF
B1			Move OPT_FAN_RPM and FAN_RPM to SYSMAX
B1			Replace MXP with QSFPDD1x1 on right side
B1			Sawp lane order to support (2x50G PAM4) 100G on QSFPDD2x1 and QSFPDD1x2 ports
B1			Move S10_2V5 power sequence
B1			Silab clock chip use AC coupling to E-tile reference clock pins

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