Visual Designer Studio Release Notes (Beta Release)

Quartus Prime Pro Software

Last updated: **2025-09-26**

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1.0 Release Notes for Visual Designer Studio

The following documents the known issues and limitations for the Visual Designer Studio Beta Release in Quartus Prime Pro version 25.3. For more information on how to use Visual Designer Studio, please refer to the Visual Designer Studio User Guide.

1.1 Known Issues

The following known issues and limitations exist in this version of Visual Designer Studio (VDS):

ID Number	Description	Workaround	Status
Visual Designer Studio User Interface			
-	Visual Designer Studio only supports Agilex 3 and Agilex 5 Devices in Quartus Prime Pro software and cannot be used for Arria 10, Stratix 10 or Agilex 7 designs.	No Workaround	Available in future release.
-	Visual Designer Studio is not available for Quartus Prime Standard software.	No Workaround	No plans to include in a future release.
16028624786	If you attempt to close the Visual Designer Studio while it is initially loading, it may cause VDS not to respond and you will be asked to terminate the application. Afterwards, Quartus might close unexpectedly as well.	Reopen Quartus Prime Pro.	Fixed in a future release.

-	Clicking on a Visual Designer Studio qsys system file in the Quartus Project Navigator launches legacy Platform Designer, instead of Visual Designer Studio.	You must use the "Load System" button in the Visual Designer Studio tool to open the qsys system.	Fixed in a future release.
14025686959	When running Design Rules Check (DRC), any dangling connections in your system are listed as a DRC warning. The DRC tool will not automatically fix these connections.	By selecting the warning instance in the DRC window, the offending component will be highlighted. From here you can select and delete each connection, perform system validation and save to solve warnings.	Fixed in future release.
14024478646	If you edit a comment applied to a component in Visual Designer Studio canvas, the change will not display in the TCL command window.	No Workaround	Fixed in future release.
16028536198	There is no undo or redo button in the Visual Designer Studio Canvas editor.	You must manually remove or add changes you have previously made.	Fixed in a future version.
System Creation			
14024571809	You cannot import a legacy qsys system into the new Visual Designer Studio Tool.	No Workaround	Available in a future release.
14023806009	A qsys system generated in Visual Designer Studio cannot automatically be assigned as a top level entity.	You need to make the TOP_LEVEL_ENTITY assignment in the qsf file.	Fixed in a future release.

16027322627	If simulation is enabled in your project, and you create and generate a new system using Visual Designer Studio, the source files and qsf will not be updated in your project or Project Navigator view in Quartus.	Add the source files manually to your project.	Fixed in future release.
14023953881	If you create a Visual Designer Studio project in Quartus after already working with a different system in a different project, Quartus will still display the system from the previous project in the **Open System** view.	If your new project has a system named the same as your previous project, you will need to close and reopen Quartus for the appropriate system to be recognized. If your new project does not have systems of the same name, the extraneous systems showing in the display can be ignored.	Fixed in future release.
14024861393	Visual Designer Studio does not support the ability for an exported input to fanout to multiple component inputs.	You must manually instantiate bridges to handle fanout.	Fixed in future release.
14024879300	Visual Designer Studio currently does not allow you to import or re-import a system with the same name as an existing system and reports an error indicating that name already exists.	Deleting your system in your project directory will allow you to complete a reimport of the design.	Fixed in a future release.

16028533931	If you delete a component from a generated system in the Visual Designer Studio Canvas, it is not automatically deleted from your project directory in Quartus and can cause compilation errors.	If you delete a component in the VDS canvas, you must also manually delete it from the Project Navigator from the Quartus window.	Fixed in a future release.
-	If you open a new system and then source a tcl script that was generated with vds::export_system, the script will error out due to the "vds:: create_system" command in the first line of code.	Comment out the vds::create_system line if you already have a system open.	Fixed in future release.
14025887963	If you have created a project using Visual Designer Suite and initiate a new Visual Designer Suite project without closing Quartus Prime Pro, you may see systems from your previous designs when you select the "Open System" icon in the left tool bar or right-click on the "Add System" menu selection in the canvas.	To have a clean view, please close Quartus and reopen it before starting a new design.	Fixed in a future release.
-	Quartus Archiver does not work within Visual Designer Studio.	No Workaround	Fixed in a future release.
18041750828	If you add an IPX file to your project and attempt to add one of these new IPs to the canvas,	To remedy this issue, restart Quartus after adding IPX file.	Fixed in future release.

	Quartus may quit unexpectedly.		
16025992412	If a DRC returns a SYNCWARNING stating "System Information doesn't match requirements of IP. Double-click to open System info tab", the System Information tab will not open up if you double-click it.	Open the System Information tab manually.	Fixed in future release.
16027355061	If a DRC returns a SYNCWARNING stating "Warning found in IP Parameterization", you cannot click on the warning to identify the error.	You must select the offending IP, open up the IP GUI, and modify any parameter to force the warning display message to appear. After the message appears and you correct the issue, return the parameter you changed back to its original state.	Fixed in a future version.
14024973812	Importing an HPS subsystem design into Visual Designer Studio may report SYNCWARNINGS during IP generation.	These warnings can be ignored.	Fixed in future release.
Netlist Navigator			
16028536411	Exported signals that are selected in the Netlist Navigator do not consistently get highlighted in the Block Diagram Canvas view.	No Workaround	Fixed in a future release.
Address Map Viewer			

-	Global Address view can display all the addresses for a hierarchical system, but you cannot edit this view.	To edit addresses within a hierarchy, you must select each sub-hierarchy view and edit the individual sub-hierarchy address maps.	Fixed in future release.
16028341222	Using the **Auto Assign System** button in the Address Map Viewer does not resolve all conflicts.	You may need to manually edit the addresses in the Address Map Viewer to resolve address overlap conflicts.	Fixed in a future release.
RTL Import			
14025089044	If an imported RTL component is deleted, the files remain within the project folder.	If you delete an imported RTL component in Visual Designer Studio, you must manually delete all the files in your system project folder.	Fixed in future release.
14025928045	If you import RTL into your system with the same entity or module definition and then make a change to that RTL, you will see a red banner that asks you to update your RTL in VDS because "One or more RTL blocks have changed since last compilation." If you select the **Update** button, VDS may report an error stating "Failed to execute command: update_cells. Please refer to the Quartus Messages window for more details." This error occurs	As a best practice, export the tcl file for your system	

	because the tool cannot reconcile changes to multiple RTL instances.		
System Referencing & Hierarchy			
22021138695	If you rename a system within a hierarchy, all addresses for the IP in the hierarchy are removed in the address map.	No Workaround; renaming of hierarchy cells is not supported.	Fixed in future release.
-	Moving components in and out of an existing hierarchy within the canvas is not supported.	No Workaround	Available in future release.
16028641245	If you create multiple hierarchical systems with components that have similar instance names, the error "Failed to create instance because instance named '' already exists" will be reported if you export your design to tcl and subsequently try to source it. For example, if you had multiple instances named "clock_bridge_0" in your nested hierarchy you would see this error.	Ensure you give different names to similar component instances in your nested hierarchy to prevent this error.	Fixed in a future release.
16028545260	If you preassign addresses to components and then create a hierarchy from those components, Visual Designer Studio clears address assignments for the components in the	You must run auto-assign in the address map editor for the created hierarchy or manually reassign the addresses to the components in the hierarchy.	Fixed in a future release.

	new hierarchy and reports address map errors during generation.		
16028530509	Non-overlapping interrupt values in a hierarchy are not automatically assigned when components with interrupt signals are instantiated in the VDS Block Designer canvas.	You must select the **Interrupt Editor** icon in the left tool bar and assign non-overlapping interrupt numbers manually.	Fixed in a future release.
16028533109	If you recreate a hierarchical qsys system by sourcing a tcl file, any vds::set_interrupt_irq command in the file will be assigned IRQ 0 regardless of the actual number assigned.	You must manually modify the IRQ value in the **Interrupt Editor** after the system is created.	Fixed in a future release.
18043449504	If you select the "Dive into packaged subsystem" button for the External Memory Interfaces for HPS Intel FPGA IP or the External Memory Interface for FPGA IP for Agilex devices, you may experience unexpected results.	Do not use the "Dive into packaged subsystem" button for these IP. Instead, use TCL commands to modify parameters. Refer to the Agilex 5 HPS-EMIF Tutorial Example Design Guide Using Visual Designer Studio for directions on how to do this.	Fixed in future release.

1.2 Important Notes about Hierarchy Creation

There are some special tips to note about hierarchy creation that are explained in our other user guides but are also referenced here as known limitations:

1. Clock and other interfaces crossing hierarchy boundaries require bridges to be inserted within the hierarchy.
2. Hierarchy ports are not optimized. Individual hierarchy ports are created for every sink instead of using consolidated ports.

3. Parent and child systems in nested hierarchies must be created in the same directory location. Because paths for .ip and qsys files of all resources (IP/System) used in a parent system are relative to the parent .qsys file, the system cannot resolve nested relative locations.

1.3 Notice and Disclaimers

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2.0 Document Revision History

Date	Version	Changes
2025-09-26	1.0	Initial release.