NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321502-A
Gerber Files	110-0321502-A
PCB Design Files	120-0321502-A
Assembly Drawing	130-0321502-A
Fab Drawing	140-0321502-A
Schematic Drawing	150-0321502-A
PCB Film	160-0321502-A
Bill of Materials	170-0321502-A
Schematic Design Files	180-0321502-A
Functional Specification	210-0321502-A
PCB Layout Guidelines	220-0321502-A
Assembly Rework	320-0321502-A

Agilex™ F-Series Transceiver-SoC Development Kit

REV	DATE	PAGES	DESCRIPTION
A	03 May. 2019	All	Modified from150-0321501-A1

PAGE	DESCRIPTION	PAGE	DESCRIPTION	PAGE	DESCRIPTION	PAGE	DESCRIPTION
01	Title, Notes, Catalog	22	FPGA Bank - 3A	43	PWRUB2MAX 1	64	PWR - FPGA VCCPT 1.8V
02	Block Diagram	23	FPGA Bank - HPS	44	PWRUB2MAX 2	65	PWR - FPGA VCCIO 1.2V
03	Power Tree & Sequence	24	FPGA Bank - 9A E-tile	45	PWRUB2MAX 3	66	PWR - FPGA VCCL_HPS 0.9V
04	FPGA Power Group	25	FPGA Bank - 10A P-tile	46	SYSMAX 1	67	PWR - FPGA VCCL_SDM 0.8V
05	Reset Topology	26	FPGA Power 1	47	SYSMAX 2	68	PWR - FPGA VCCH_GXE 1.1V
06	Clock Tree, Bank Usage	27	FPGA Power 2	48	SYSMAX 3	69	PWR - FPGA VCCIO 1.8V
07	I2C Chain	28	FPGA GND 1	49	Temp Sense/Fan	70	PWR - FPGA VCCIO 1.5V
08	JTAG Chain	29	FPGA GND 2	50	Power Monitors	71	PWR - FPGA VCCCLK_GXE 2.5V
09	PWRUB2MAX Functional Diagram	30	FPGA NC/DNU	51	Clock 1	72	PWR - FPGA VCCFUSEWR 2.4V
10	SYSMAX Function Diagram	31	260 Pin SO-DIMM	52	Clock 2	73	PWR - SODIMM VTT 0.6V
11	SODIMM Pin Table	32	DDR4 Component 1	53	CLOCK CLEANER	74	PWR - SODIMMVDD 1.2V-1.35V
12	Power Sequence	33	DDR4 Component 2	54	I2C And PMBUS	75	PWR - DDR4 VTT 0.6V
13	E-tile Pin Swap Map	34	DDR4 Comp Termination	55	PWR - POWER INPUT	76	PWR - 1.8V
14	FPGA Bank - SDM	35	FLASH Daughter Cards	56	PWR - 3.3V_PRE	77	PWR - 2.5V
15	FPGA Bank - 2D	36	QSFPDD1x1	57	PWR - 12V	78	PWR - 1.2V
16	FPGA Bank - 2C	37	zQSFP	58	PWR - BIAS	79	FPGA Decoupling Caps 1
17	FPGA Bank - 2B	38	MXP Connectors	59	PWR - 3.3V	80	FPGA Decoupling Caps 2
18	FPGA Bank - 2A	39	PCIe RC Connector	60	PWR - FPGA VCC VID 1	81	FPGA Decoupling Caps 3
19	FPGA Bank - 3D	40	10/100/1000 Ethernet PHY	61	PWR - FPGA VCC VID 2		
20	FPGA Bank - 3C	41	FPGA Test IOs	62	PWR - FPGA VCC VID 3		
21	FPGA Bank - 3B	42	On Board USB BLASTER II	63	PWR - FPGA VCCH 0.9V		

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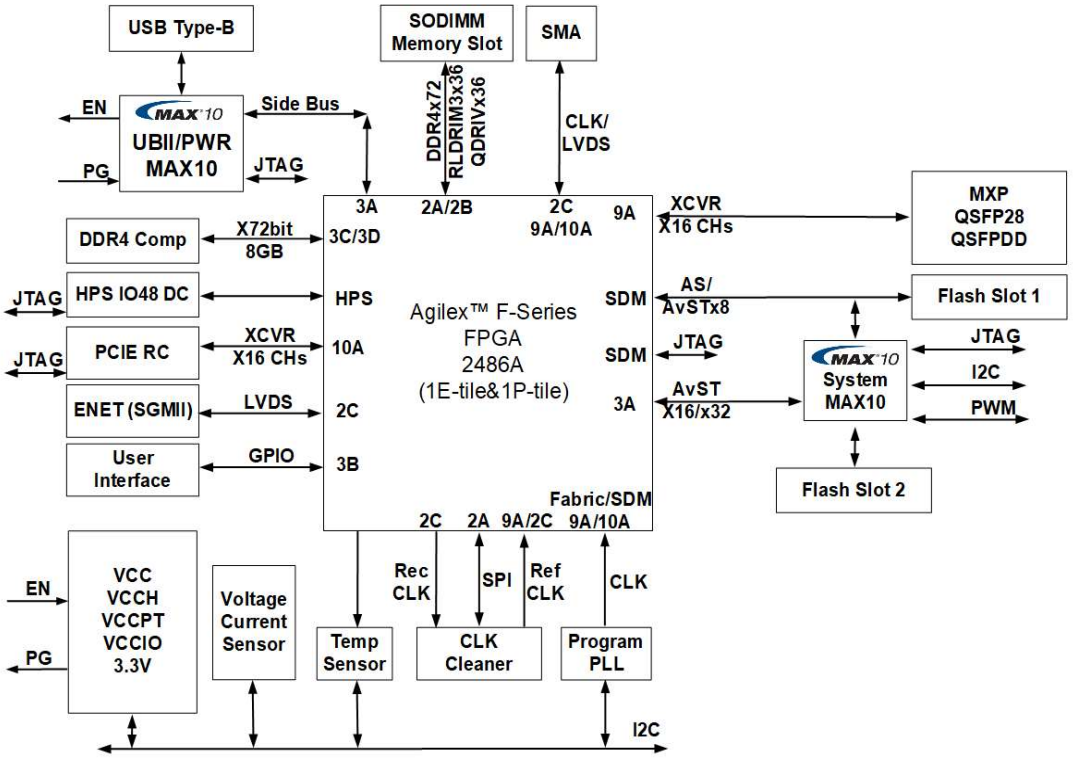
Block Diagram



E-TILE: 9A 16CHs/9REFCLK
P-TILE: 10A 16CHs/5REFCLK
IO96: 2A/2B/2C/2D/3A/3B/3C/3D
TSD: CORE/E-TILE/P-TILE
HPS: 48 IOs
SDM: 17 IOs

Reuse the Boot Flash DC and HPS IO48 DC in S10 Gen
Flash slot 1 for FPGA AS configuration and HPS initial boot based on NAND/QSPI/SD/eMMC DC
Flash slot 2 for System MAX10 AvSTx8/16/32 configuration based on NAND/QSPI/SD/eMMC DCs
Combine flash slot 1 and 2 for System MAX10 AvSTx16/x32 configuration based on CFI NOR DC
HPS IO48 DC for HPS following boot and function expansion
UBII/PWR MAX10 manages JTAG, Side Bus, power sequence and over temp. protection, hidden for customer
System MAX handles AvST configuration, I2C manage (clock/power/monitor ICs) and fan control, open for customer
Design SODIMM memory DCs for RLDRAM3 and QDRIV based on IO96A rules

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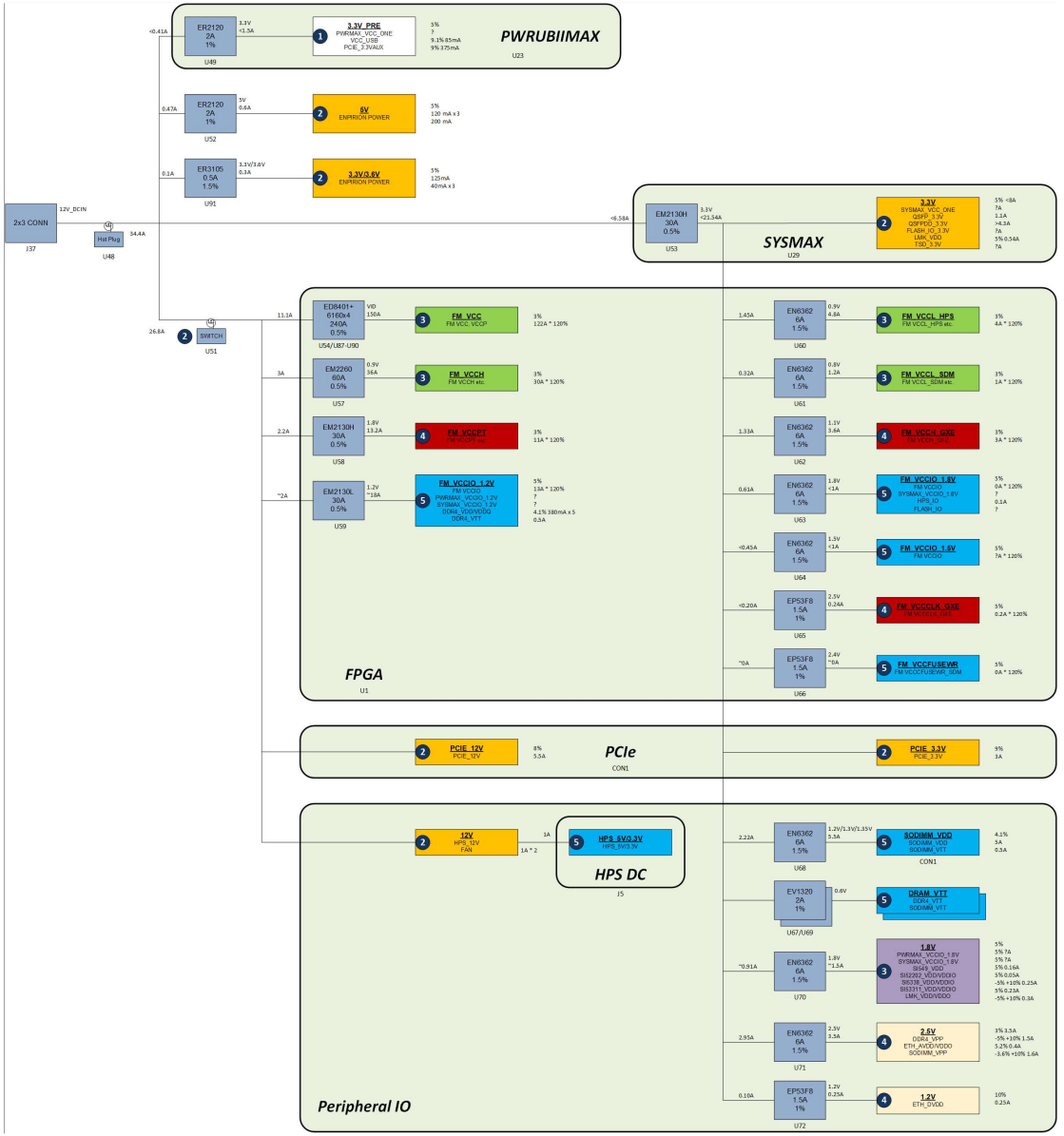
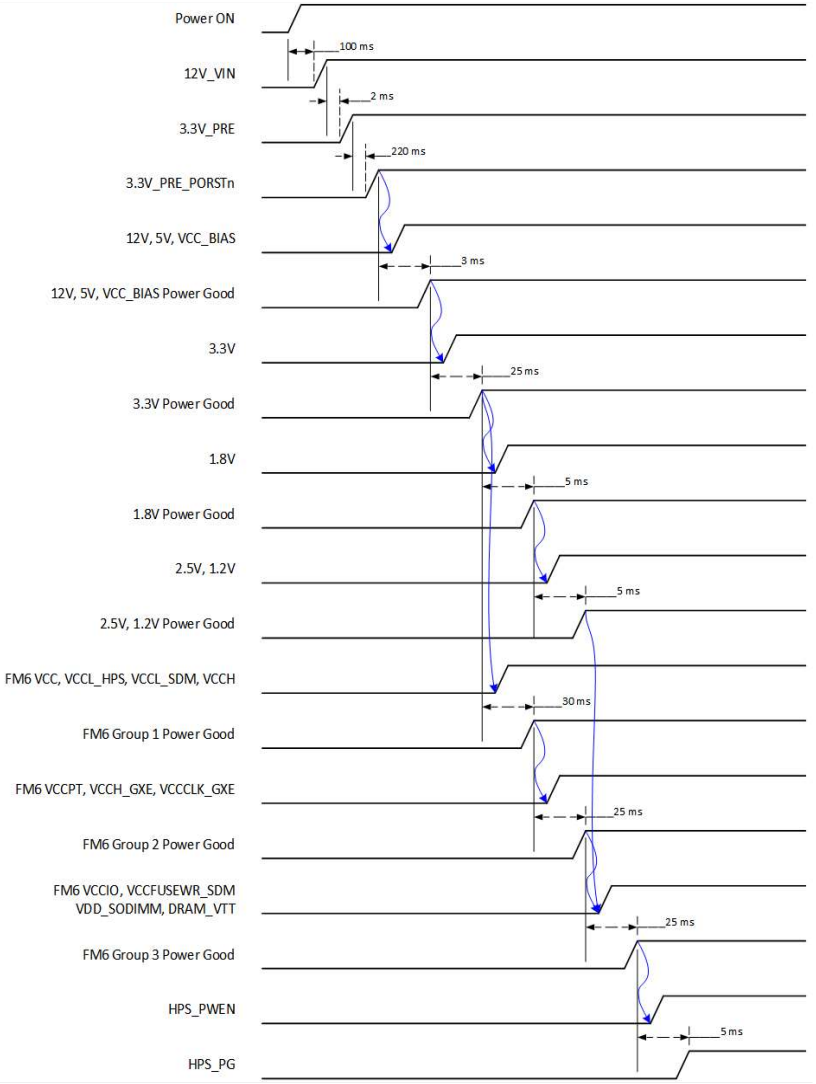
Power Tree & Sequence





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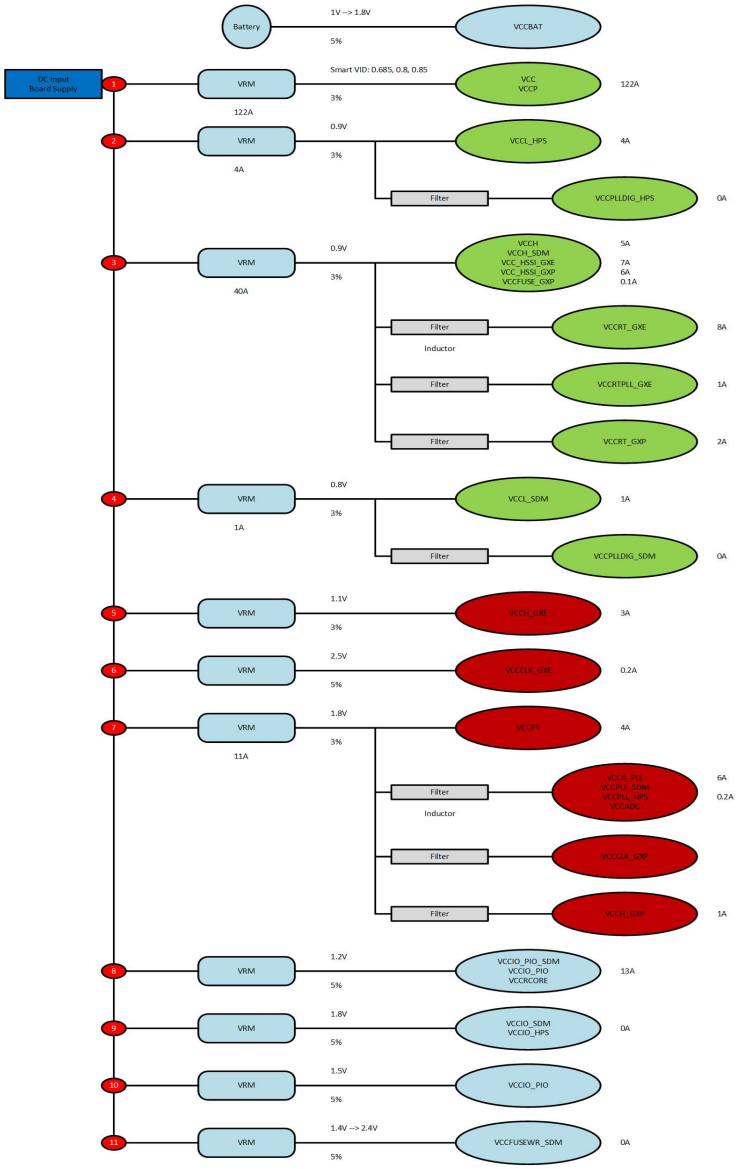
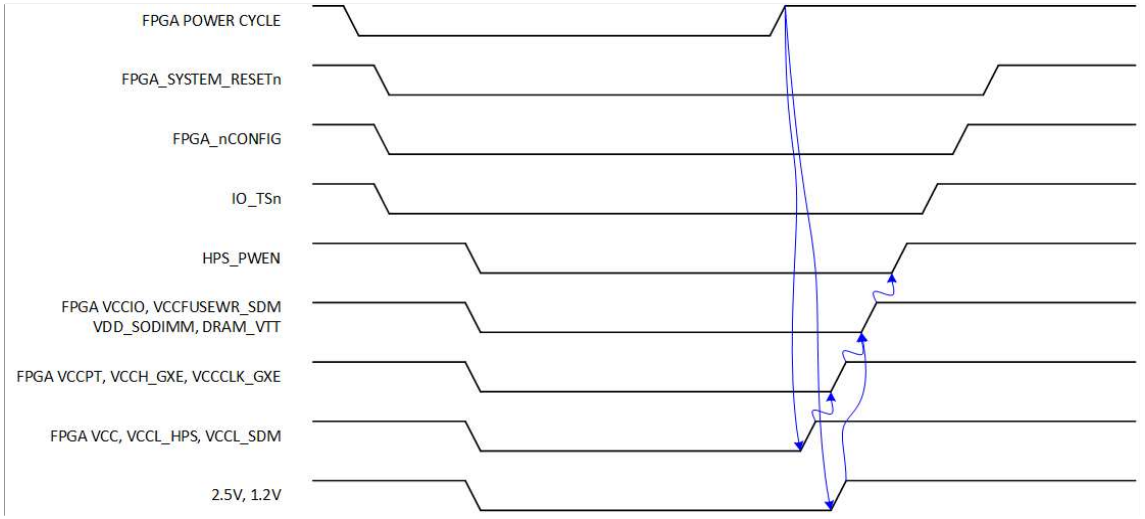
FPGA Power Group





FPGA Power Recycle

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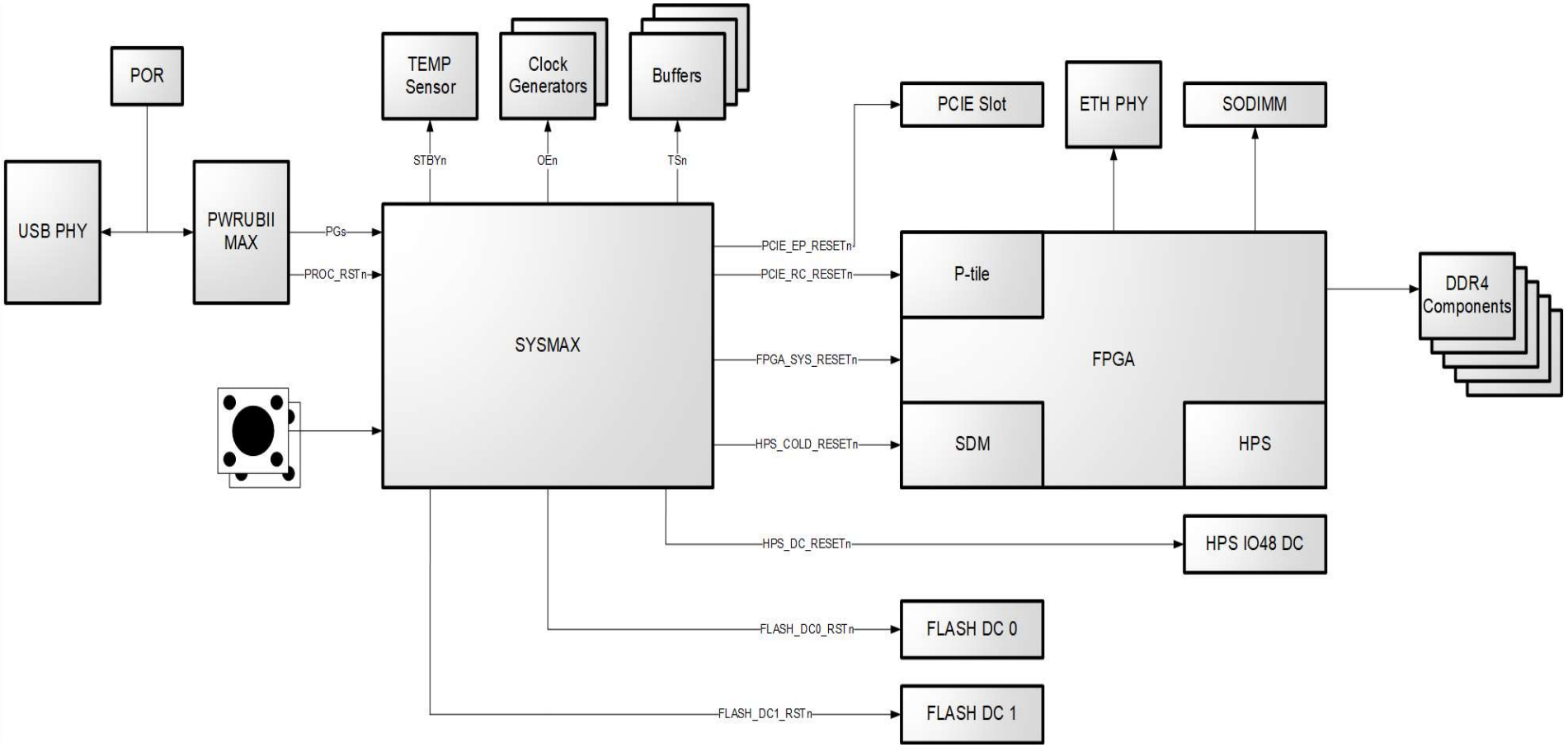
Reset Topology



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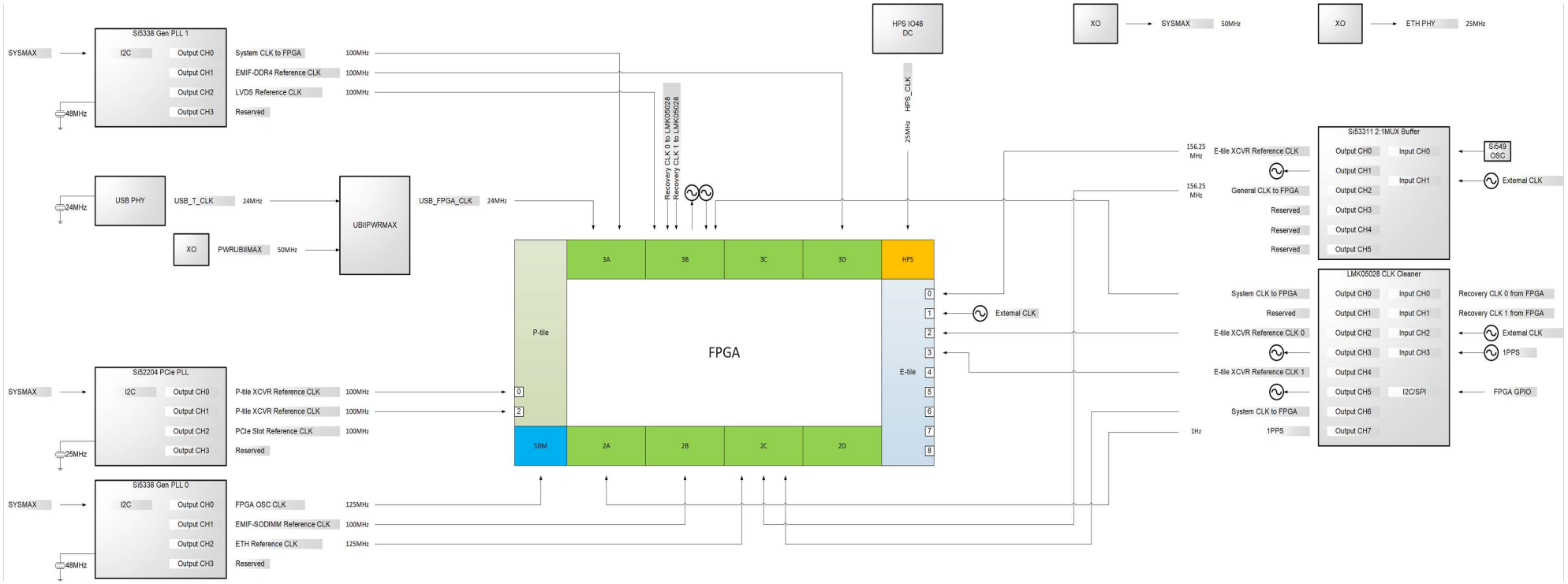
Clock Tree



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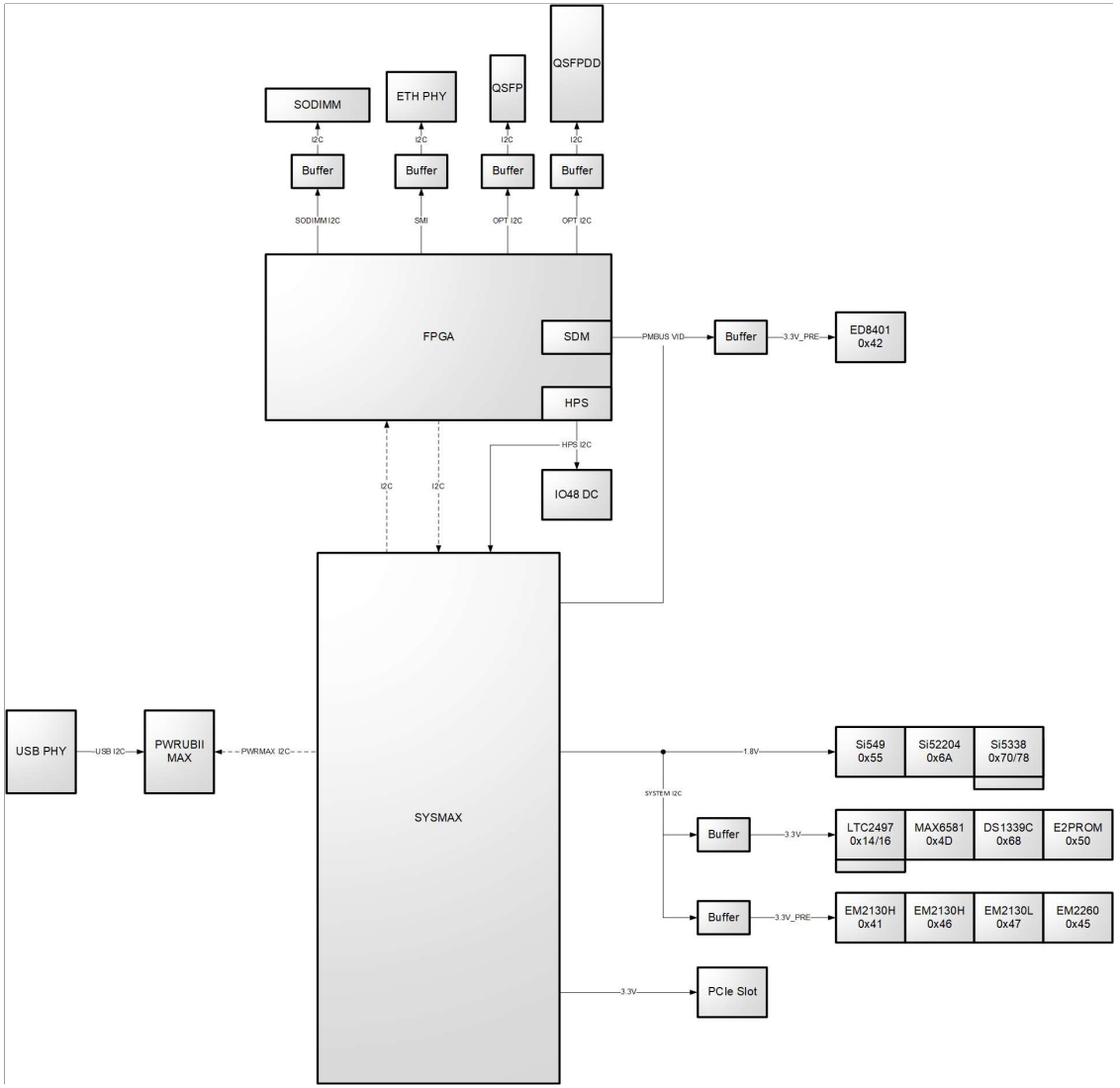
I2C Bus Topology



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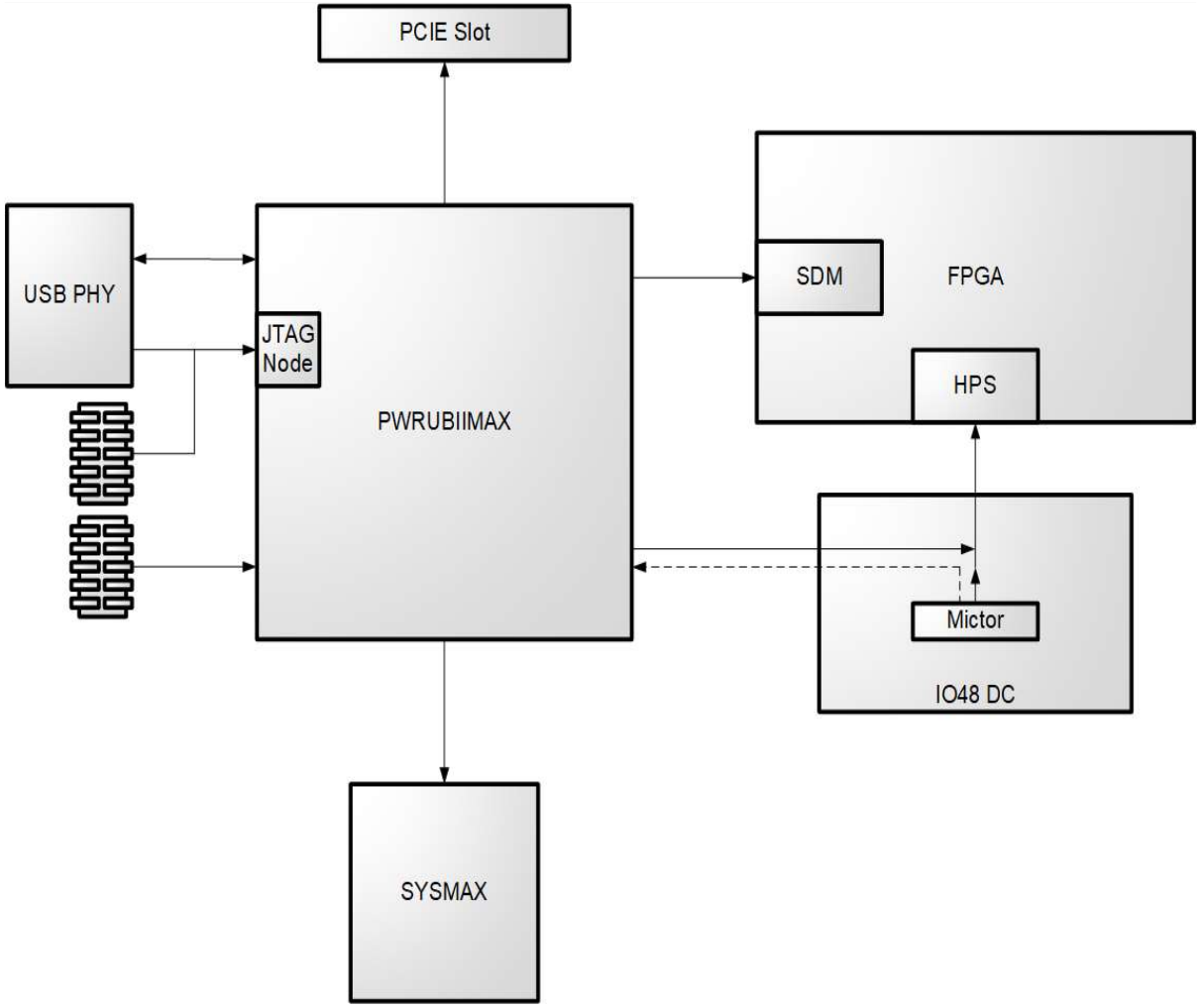
JTAG Chain Topology



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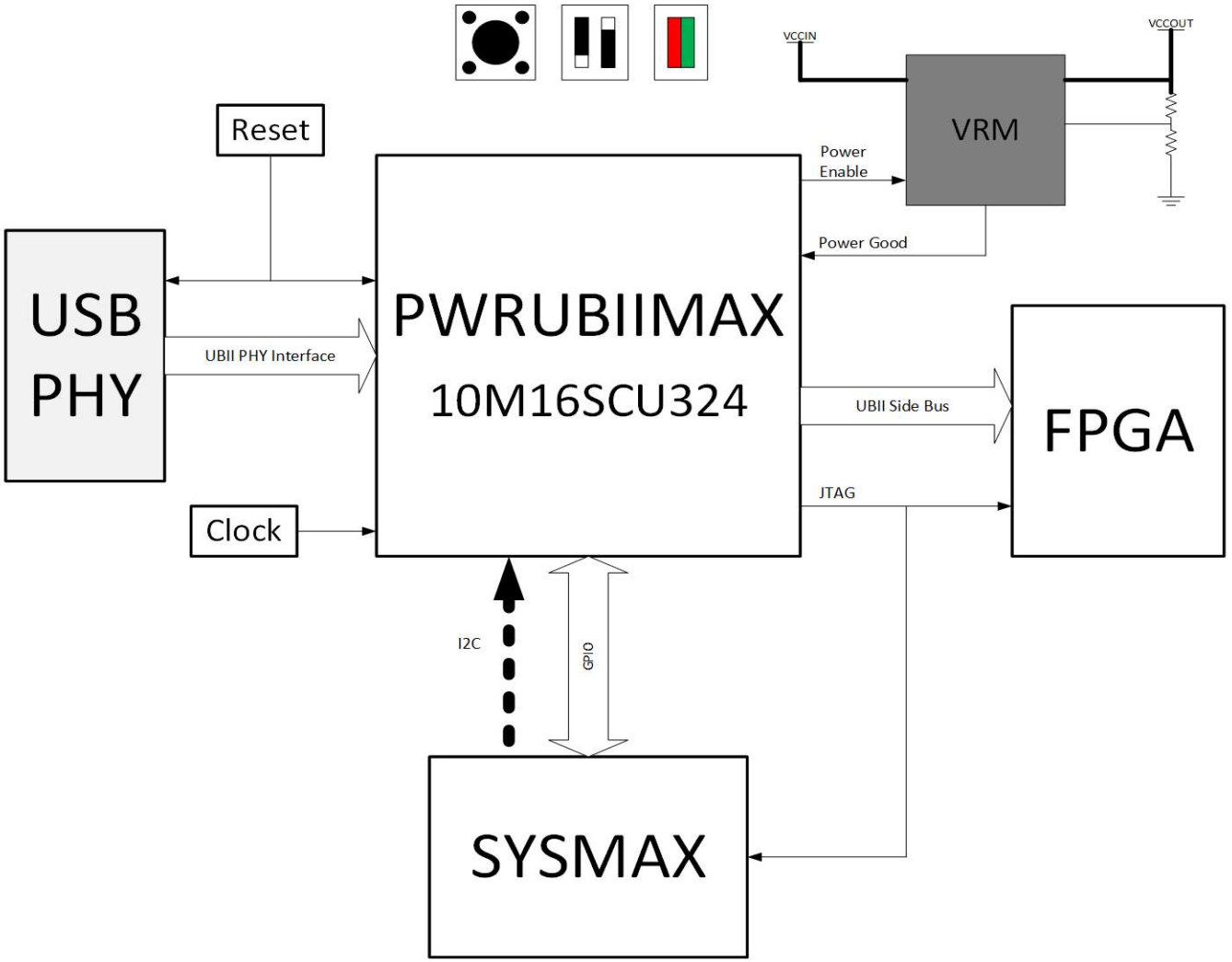
PWRUBIIMAX Diagram



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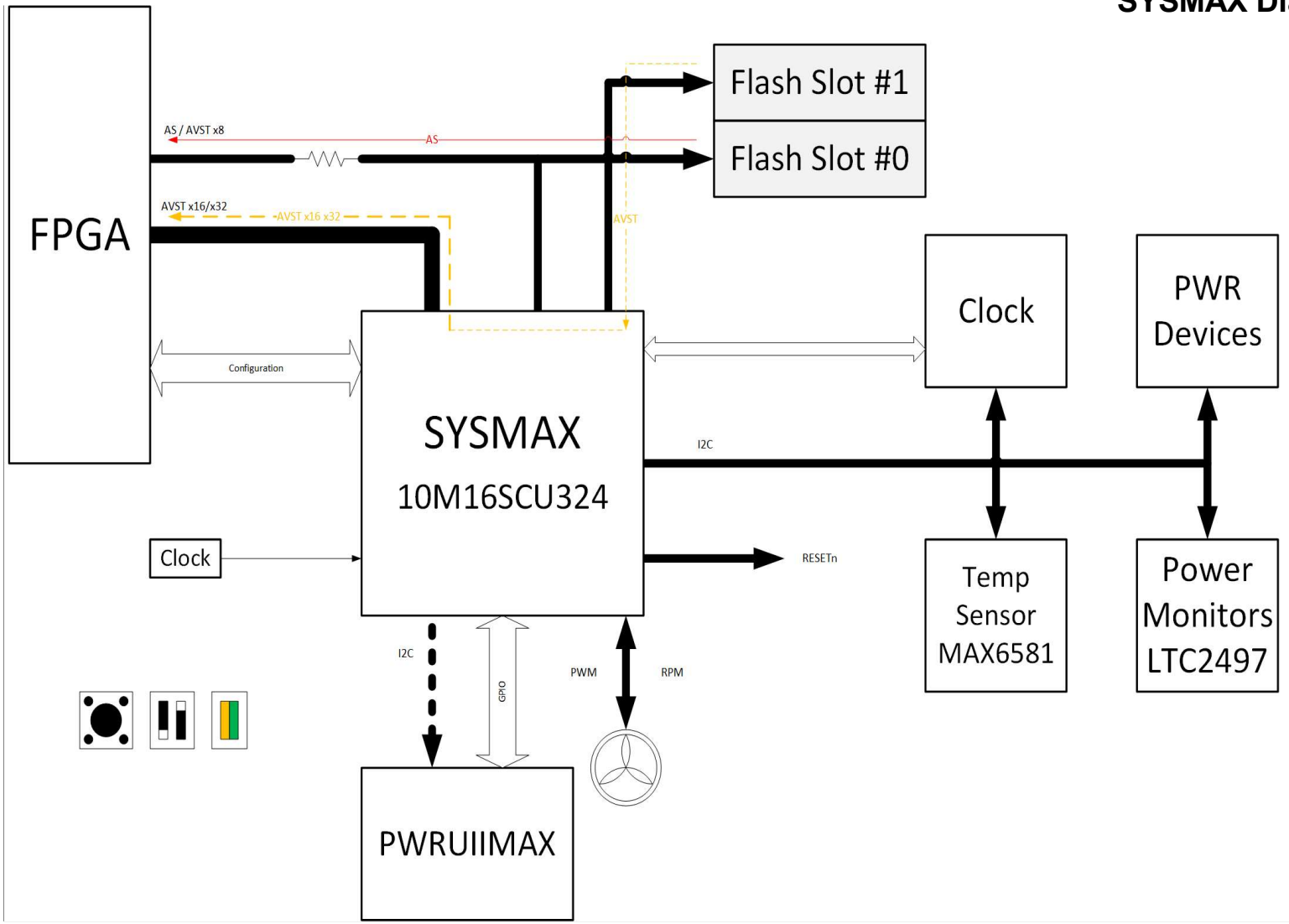
SYSMAX Diagram



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SODIMM Pin Table

DDR4 x72 (DQS x8 Groups) FM6	RLDRAM3 x36 FM	QDRIV x36 FM	HiLo Pin Name	260pin SODIMM Pin Number	SODIMM function	Lane	DDR4 x72 (DQS x8 Groups) FM6	RLDRAM3 x36 FM	QDRIV x36 FM	HiLo Pin Name	260pin SODIMM Pin Number	SODIMM function	Lane	DDR4 x72 (DQS x8 Groups) FM6	RLDRAM3 x36 FM	QDRIV x36 FM	HiLo Pin Name	260pin SODIMM Pin Number	SODIMM function	Lane
DQ24	DQ9	DQA0	MEM_DQA[24]	70	DQ24	00_00	BG1	BA3	RWAn	MEM_ADDR_CMD[00]	113	BG1	04_00	DQS6	DQ0	DQB0	MEM_DQB[24]	237	DQS6	08_00
DQ25	DQ10	DQA1	MEM_DQA[25]	71	DQ25	00_01	RESETn	RESETn	RWBn	MEM_ADDR_CMD[01]	108	RESETn	04_01	DQ57	DQ1	DQB1	MEM_DQB[25]	236	DQ57	08_01
DQ26	DQ11	DQA2	MEM_DQA[26]	83	DQ26	00_02	CSn0	CSn0	LDAn	MEM_ADDR_CMD[02]	149	CS0n	04_02	DQ58	DQ2	DQB2	MEM_DQB[26]	249	DQ58	08_02
DQ27	DQ12	DQA3	MEM_DQA[27]	84	DQ27	00_03	ACTn	CSn1	LDBn	MEM_ADDR_CMD[03]	114	ACTn	04_03	DQ59	DQ3	DQB3	MEM_DQB[27]	250	DQ59	08_03
DQS_P3	QK1	QKA_P0	MEM_DQSA_P[3]	76	DQS3	00_04	ODT0	A18	CK_P	MEM_ADDR_CMD[04]	155	ODT0	04_04	DQS_P7	QK0	QKB_N0	MEM_DQSB_P[3]	242	DQS7	08_04
DQS_N3	QK1#	QKA_N0	MEM_DQSA_N[3]	74	DQS3#	00_05	ODT1/NC	A19	CK_N	MEM_ADDR_CMD[05]	161	ODT1	04_05	DQS_N7	QK0#	QKB_P0	MEM_DQSB_N[3]	240	DQS7#	08_05
DM_n3	DM1	DQA8	MEM_DMA[3]	75	DM3n/DBI3n	00_06	CKE0	A20	AINV_0	MEM_ADDR_CMD[06]	109	CKE0	04_06	DM_n7	DM0	DQB8	MEM_DMB[3]	241	DM7n/DBI7n	08_06
	DQ17	DINVA0	MEM_DQA[33]	138	CK1	00_07	CKE1/NC	WEn	CFGn	MEM_ADDR_CMD[07]	110	CKE1	04_07		DQ8	DINVB0	MEM_DQB[33]	162	C0/CS2n	08_07
DQ28	DQ13	DQA4	MEM_DQA[28]	66	DQ28	00_08	CK_P0	CK_P	A0	MEM_CLK_P	137	CK0	04_08	DQ60	DQ4	DQB4	MEM_DQB[28]	232	DQ60	08_08
DQ29	DQ14	DQA5	MEM_DQA[29]	67	DQ29	00_09	CK_N0	CK_N	A1	MEM_CLK_N	139	CK0#	04_09	DQ61	DQ5	DQB5	MEM_DQB[29]	233	DQ61	08_09
DQ30	DQ15	DQA6	MEM_DQA[30]	79	DQ30	00_10	CSn1/NC	CSn2	A2	MEM_ADDR_CMD[08]	157	CS1n	04_10	DQ62	DQ6	DQB6	MEM_DQB[30]	245	DQ62	08_10
DQ31	DQ16	DQA7	MEM_DQA[31]	80	DQ31	00_11	PARITY	REFn	A3	MEM_ADDR_CMD[09]	143	PARITY	04_11	DQ63	DQ7	DQB7	MEM_DQB[31]	246	DQ63	08_11
DQ16		DQA9	MEM_DQA[16]	50	DQ16	01_00	A0	A0	A4	MEM_ADDR_CMD[10]	144	A0	05_00	DQ48		DQB9	MEM_DQB[16]	216	DQ48	09_00
DQ17		DQA10	MEM_DQA[17]	49	DQ17	01_01	A1	A1	A5	MEM_ADDR_CMD[11]	133	A1	05_01	DQ49		DQB10	MEM_DQB[17]	215	DQ49	09_01
DQ18		DQA11	MEM_DQA[18]	62	DQ18	01_02	A2	A2	A6	MEM_ADDR_CMD[12]	132	A2	05_02	DQ50		DQB11	MEM_DQB[18]	228	DQ50	09_02
DQ19		DQA12	MEM_DQA[19]	63	DQ19	01_03	A3	A3	A7	MEM_ADDR_CMD[13]	131	A3	05_03	DQ51		DQB12	MEM_DQB[19]	229	DQ51	09_03
DQS_P2	DK1	DKA_P0	MEM_DQSA_P[2]	55	DQS2	01_04	A4	A4		MEM_ADDR_CMD[14]	128	A4	05_04	DQS_P6	DK0	DKB_P0	MEM_DQSB_P[2]	221	DQS6	09_04
DQS_N2	DK1#	DKA_N0	MEM_DQSA_N[2]	53	DQS2#	01_05	A5	A5		MEM_ADDR_CMD[15]	126	A5	05_05	DQS_N6	DK0#	DKB_N0	MEM_DQSB_N[2]	219	DQS6#	09_05
DM_n2		DQA17	MEM_DMA[2]	54	DM2n/DBI2n	01_06	A6	A6	A8	MEM_ADDR_CMD[16]	127	A6	05_06	DM_n6		DQB17	MEM_DMB[2]	220	DM6n/DBI6n	09_06
						01_07	A7	A7	RESETn	MEM_ADDR_CMD[17]	122	A7	05_07							09_07
DQ20		DQA13	MEM_DQA[20]	46	DQ20	01_08	A8	A8	A9	MEM_ADDR_CMD[18]	125	A8	05_08	DQ52		DQB13	MEM_DQB[20]	211	DQ52	09_08
DQ21		DQA14	MEM_DQA[21]	45	DQ21	01_09	A9	A9	A10	MEM_ADDR_CMD[19]	121	A9	05_09	DQ53		DQB14	MEM_DQB[21]	212	DQ53	09_09
DQ22		DQA15	MEM_DQA[22]	58	DQ22	01_10	A10/AP	A10	A11	MEM_ADDR_CMD[20]	146	A10/AP	05_10	DQ54		DQB15	MEM_DQB[22]	224	DQ54	09_10
DQ23		DQA16	MEM_DQA[23]	59	DQ23	01_11	A11	A11	A12	MEM_ADDR_CMD[21]	120	A11	05_11	DQ55		DQB16	MEM_DQB[23]	225	DQ55	09_11
DQ8	DQ27	DQA18	MEM_DQA[08]	28	DQ8	02_00	A12	A12	A13	MEM_ADDR_CMD[22]	119	A12	06_03	DQ40	DQ18	DQB18	MEM_DQB[08]	195	DQ40	10_00
DQ9	DQ28	DQA19	MEM_DQA[09]	29	DQ9	02_01	A13	A13		MEM_ADDR_CMD[23]	158	A13	06_04	DQ41	DQ19	DQB19	MEM_DQB[09]	194	DQ41	10_01
DQ10	DQ29	DQA20	MEM_DQA[10]	41	DQ10	02_02	A14/WE_n	A14		MEM_ADDR_CMD[24]	151	Wen/A14	06_05	DQ42	DQ20	DQB20	MEM_DQB[10]	207	DQ42	10_02
DQ11	DQ30	DQA21	MEM_DQA[11]	42	DQ11	02_03	A15/CAS_n	A15	A14	MEM_ADDR_CMD[25]	156	CASn/A15	06_06	DQ43	DQ21	DQB21	MEM_DQB[11]	208	DQ43	10_03
DQS_P1	QK3	QKA_P1	MEM_DQSA_P[1]	34	DQS1	02_04	A16/RAS_n	A16	PEn	MEM_ADDR_CMD[26]	152	RASn/A16	06_07	DQS_P5	QK2	QKB_N1	MEM_DQSB_P[1]	200	DQS5	10_04
DQS_N1	QK3#	QKA_N1	MEM_DQSA_N[1]	32	DQS1#	02_05	ALERTn	A17	A15	MEM_ADDR_CMD[27]	116	Alertn	06_08	DQS_N5	QK2#	QKB_P1	MEM_DQSB_N[1]	198	DQS5#	10_05
DM_n1		DQA26	MEM_DMA[1]	33	DM1n/DBI1n	02_06	BA0	BA0	A16	MEM_ADDR_CMD[28]	150	BA0	06_09	DM_n5		DQB26	MEM_DMB[1]	199	DM5n/DBI5n	10_06
	DQ35	DINVA1	MEM_DQA[32]	140	CK1#	02_07	BA1	BA1	A17	MEM_ADDR_CMD[29]	145	BA1	06_10		DQ26	DINVB1	MEM_DQB[32]	165	C1/CS3n	10_07
DQ12	DQ31	DQA22	MEM_DQA[12]	24	DQ12	02_08	BG0	BA2	A18	MEM_ADDR_CMD[30]	115	BG0	06_11	DQ44	DQ22	DQB22	MEM_DQB[12]	191	DQ44	10_08
DQ13	DQ32	DQA23	MEM_DQA[13]	25	DQ13	02_09	DQ65	CSn3	A19	MEM_DQ_ADDR_CMD[0]	104	CB7	07_00	DQ45	DQ23	DQB23	MEM_DQB[13]	190	DQ45	10_09
DQ14	DQ33	DQA24	MEM_DQA[14]	38	DQ14	02_10	DQ71		A20	MEM_DQ_ADDR_CMD[1]	105	CB3	07_01	DQ46	DQ24	DQB24	MEM_DQB[14]	203	DQ46	10_10
DQ15	DQ34	DQA25	MEM_DQA[15]	37	DQ15	02_11	DQ70		A21	MEM_DQ_ADDR_CMD[2]	101	CB2	07_02	DQ47	DQ25	DQB25	MEM_DQB[15]	204	DQ47	10_11
DQ0		DQA27	MEM_DQA[00]	8	DQ0	03_00	DQ69		A22	MEM_DQ_ADDR_CMD[3]	100	CB6	07_03	DQ32		DQB27	MEM_DQB[00]	174	DQ32	11_00
DQ1		DQA28	MEM_DQA[01]	7	DQ1	03_01	DQS_P8			MEM_DQS_ADDR_CMD_P	97	DQS8	07_04	DQ33		DQB28	MEM_DQB[01]	173	DQ33	11_01
DQ2		DQA29	MEM_DQA[02]	20	DQ2	03_02	DQS_N8			MEM_DQS_ADDR_CMD_N	95	DQS8#	07_05	DQ34		DQB29	MEM_DQB[02]	187	DQ34	11_02
DQ3		DQA30	MEM_DQA[03]	21	DQ3	03_03	DM_n8		AP	MEM_DQ_ADDR_CMD[4]	96	DM8n/DBI8n	07_06	DQ35		DQB30	MEM_DQB[03]	186	DQ35	11_03
DQS_P0		DKA_P1	MEM_DQSA_P[0]	13	DQS0	03_04							07_07	DQS_P4		DKB_P1	MEM_DQSB_P[0]	179	DQS4	11_04
DQS_N0		DKA_N1	MEM_DQSA_N[0]	11	DQS0#	03_05	DQ66		A23	MEM_DQ_ADDR_CMD[5]	88	CB4	07_08	DQS_N4		DKB_N1	MEM_DQSB_N[0]	177	DQS4#	11_05
DM_n0		DQA35	MEM_DMA[0]	12	DM0n/DBI0n	03_06	DQ67		A24	MEM_DQ_ADDR_CMD[6]	91	CB1	07_09	DM_n4		DQB35	MEM_DMB[0]	178	DM4n/DBI4n	11_06
						03_07	DQ64		LBK0n	MEM_DQ_ADDR_CMD[7]	92	CB0	07_10							11_07
DQ4		DQA31	MEM_DQA[04]	4	DQ4	03_08	DQ68		LBK1n	MEM_DQ_ADDR_CMD[8]	87	CB5	07_11	DQ36		DQB31	MEM_DQB[04]	170	DQ36	11_08
DQ5		DQA32	MEM_DQA[05]	3	DQ5	03_09								DQ37		DQB32	MEM_DQB[05]	169	DQ37	11_09
DQ6		DQA33	MEM_DQA[06]	16	DQ6	03_10								DQ38		DQB33	MEM_DQB[06]	183	DQ38	11_10
DQ7		DQA34	MEM_DQA[07]	17	DQ7	03_11				CONFIG0/Card TYPE	134	EVENTn		DQ39		DQB34	MEM_DQB[07]	182	DQ39	11_11

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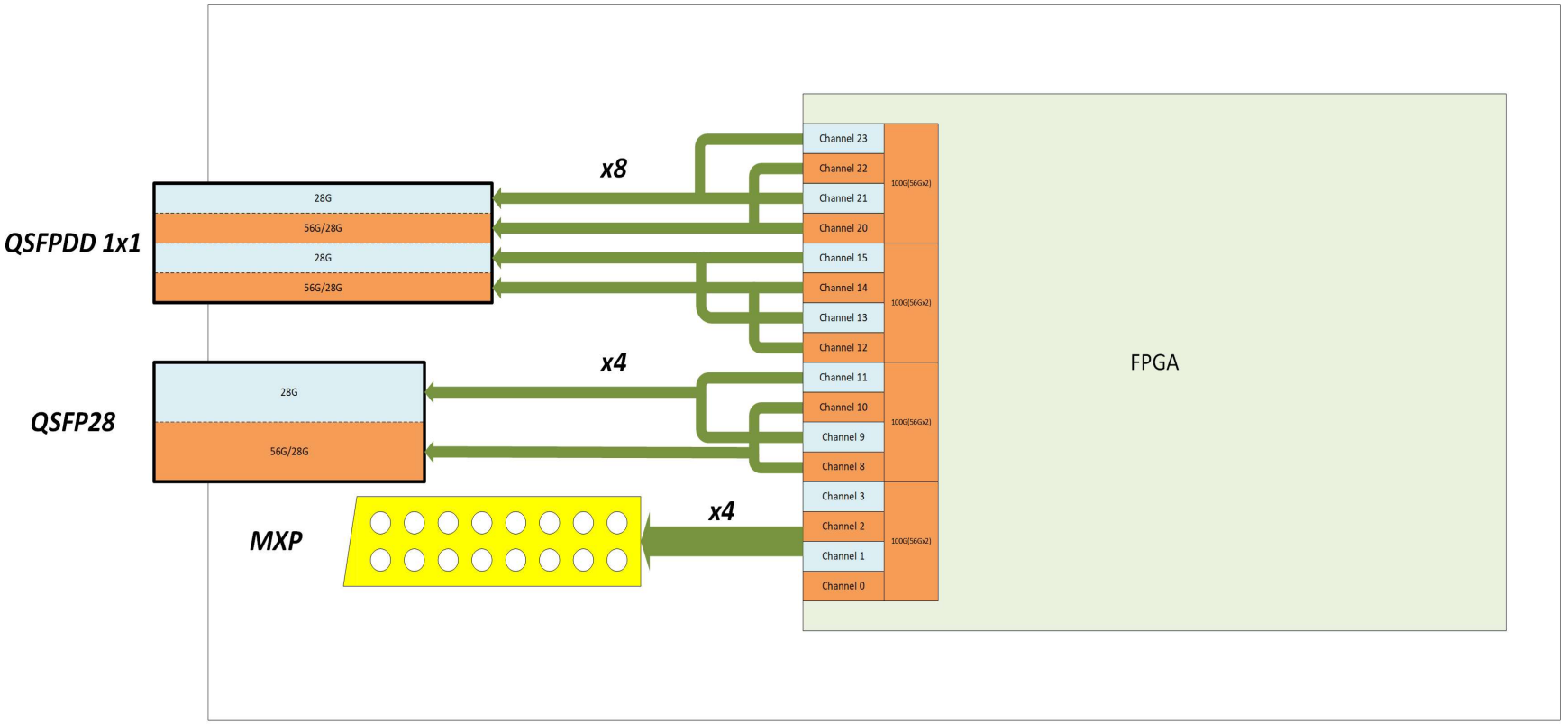
E-tile Pin Assignment



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FPGA Configuration Settings

CONFIGURATION MODE		MSEL[2:0]
Passive	AVSTx32	000
	AVSTx16	101
	AVSTx8	110
	JTAG	111
	CvP	001
Active	SD MMC	100
	AS - Fast	001
	AS - Normal	011

SDM Pins	MSEL Functions	Configuration Source Function				
		AVSTx8	AS	SD/MMC	AVSTx16	AVSTx32
SDM_IO0		PWR_SCL	PWR_SCL	PWR_SCL	PWR_SCL	PWR_SCL
SDM_IO1		DATA2	DATA1	DATA1		
SDM_IO2		DATA0	CLK	DATA0		
SDM_IO3		DATA3	DATA2	DATA2		
SDM_IO4		DATA1	DATA0	CMD		
SDM_IO5	MSEL0	HPS_CRSTn	nCSO0	CCLK		
SDM_IO6		DATA4	DATA3	DATA3		
SDM_IO7	MSEL1		nCSO2			
SDM_IO8		READY	nCSO3	DATA4		
SDM_IO9	MSEL2		nCSO1			
SDM_IO10		DATA7		DATA7		
SDM_IO11		VALID	HPS_CRSTn	HPS_CRSTn	HPS_CRSTn	HPS_CRSTn
SDM_IO12		PWR_SDA	PWR_SDA	PWR_SDA	PWR_SDA	PWR_SDA
SDM_IO13		DATA5		DATA5		
SDM_IO14		CLK				
SDM_IO15		DATA6		DATA6		
SDM_IO16		CFG_DONE	CFG_DONE	CFG_DONE	CFG_DONE	CFG_DONE

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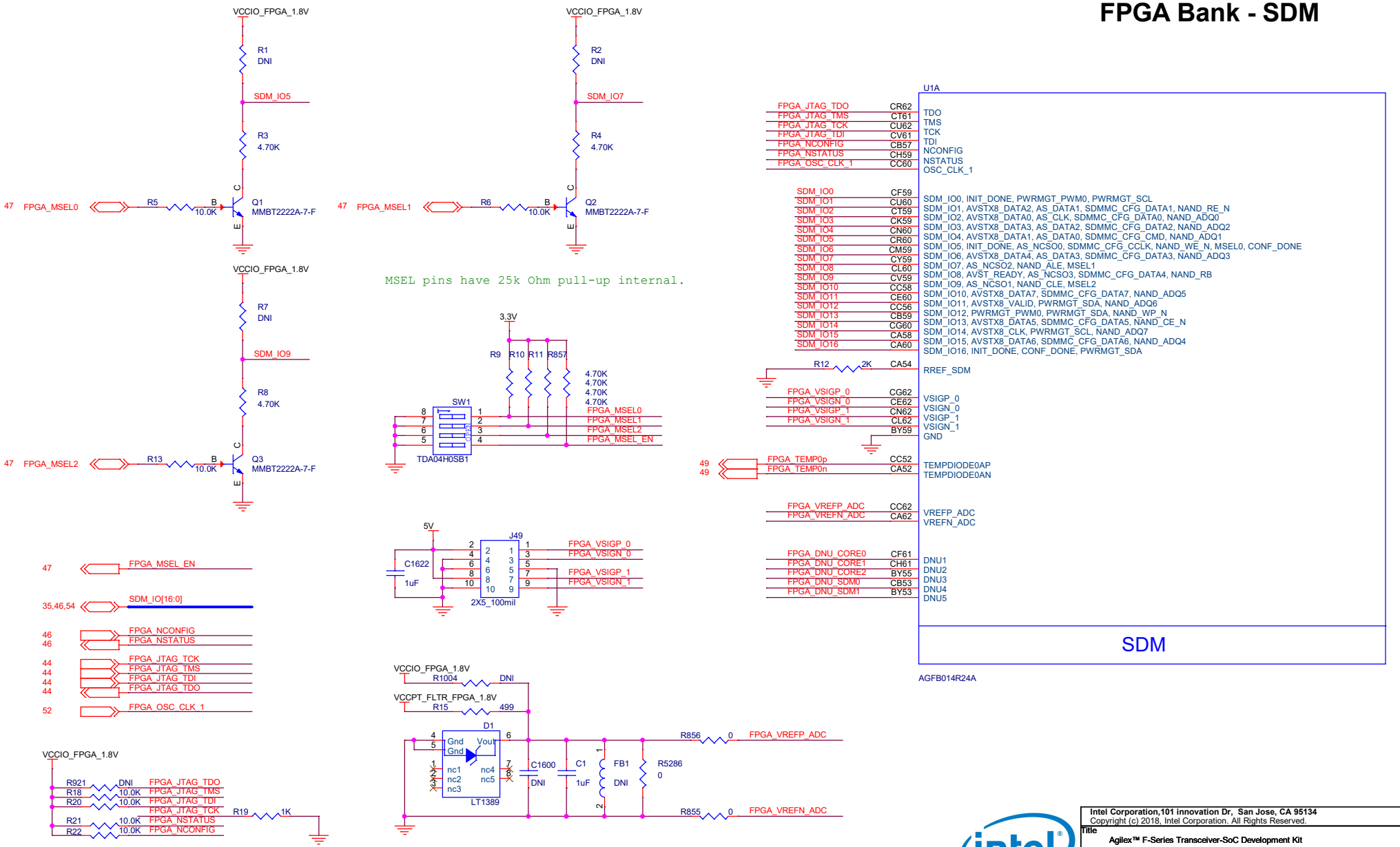
FPGA Bank - SDM



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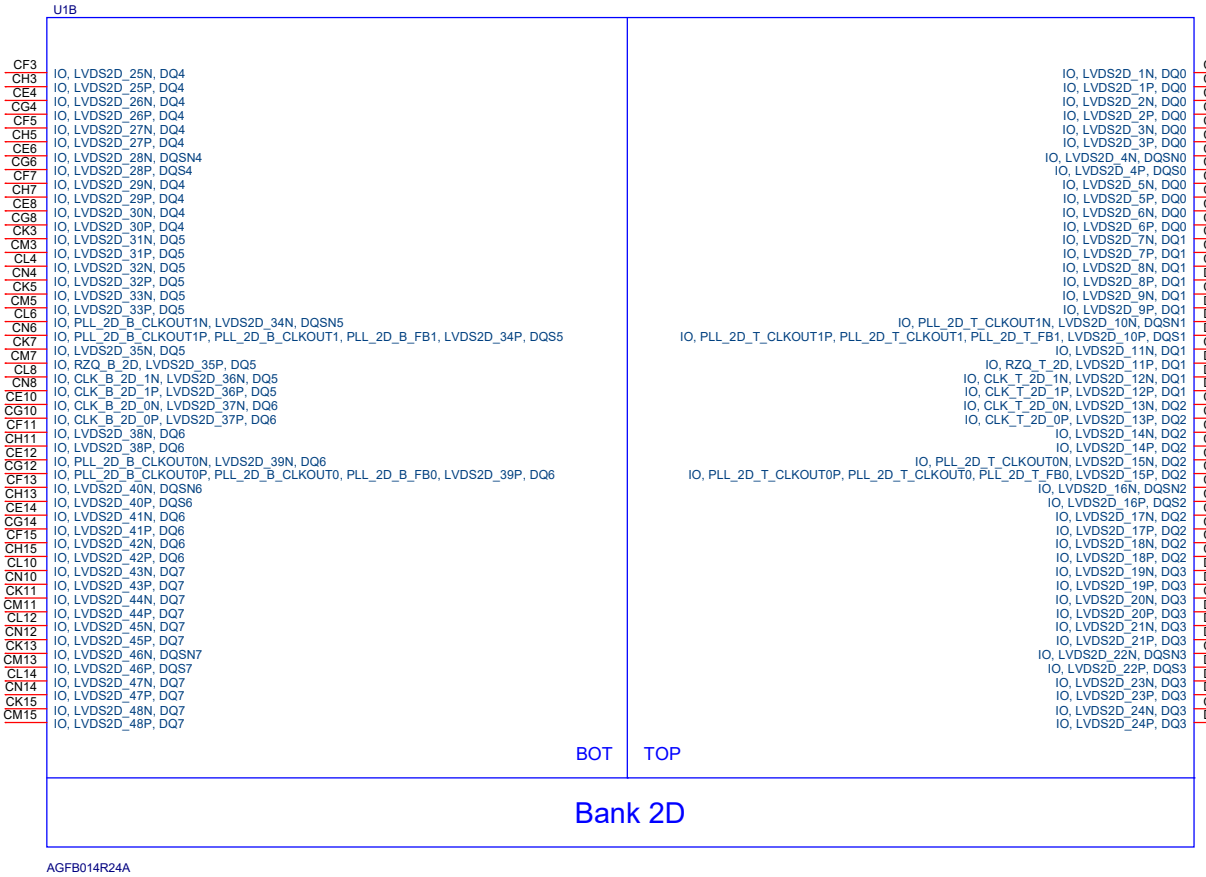
FPGA Bank - 2D



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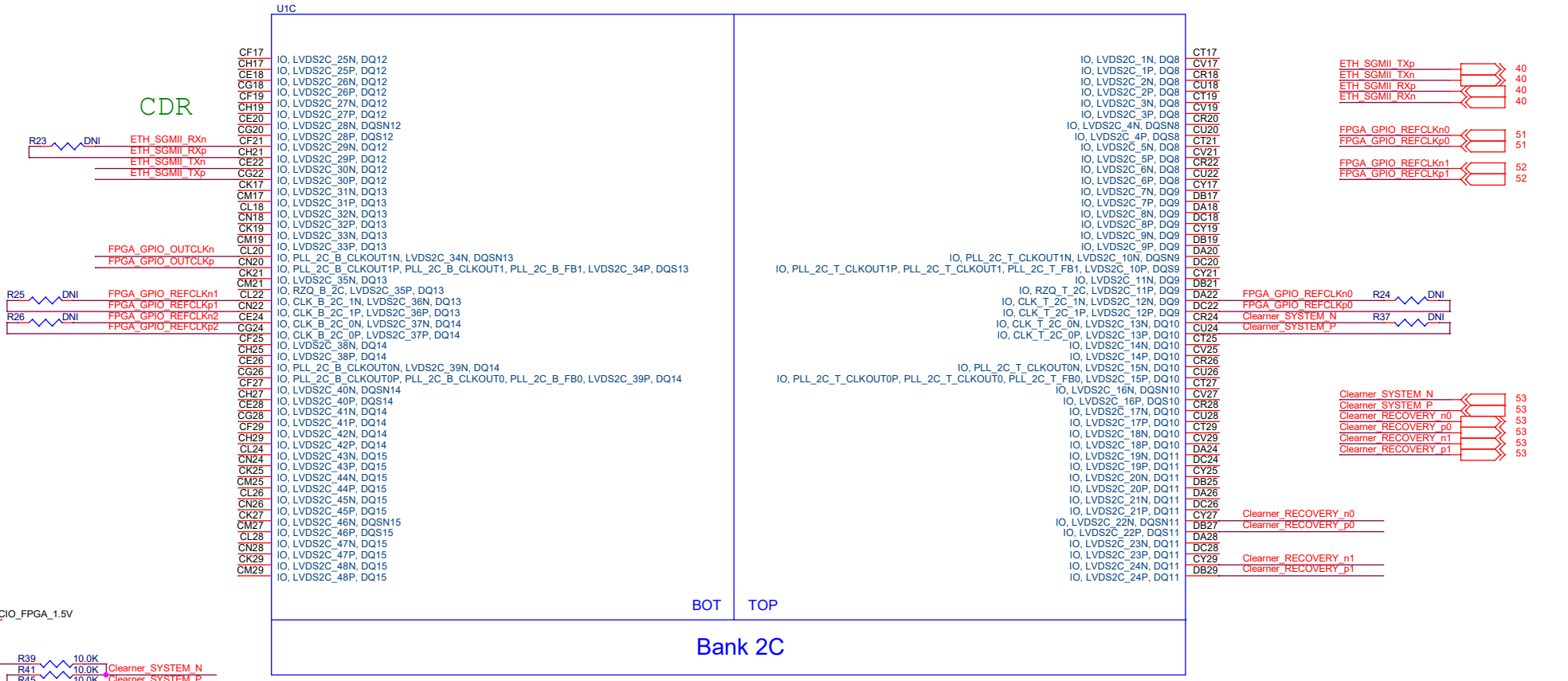
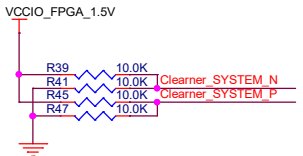
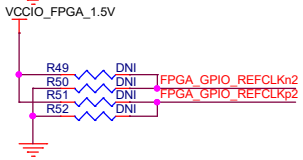
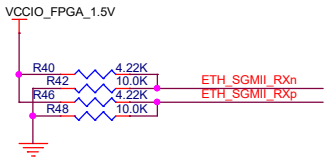
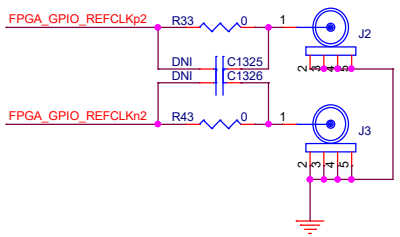
FPGA Bank - 2C

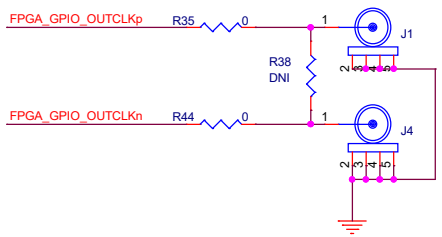


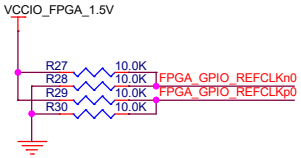


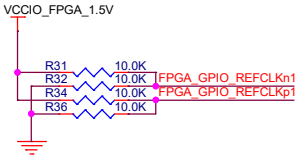












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FPGA Bank - 2B

52 SODIMM_REFCLKn
52 SODIMM_REFCLKp
31 MEM_CLKn
31 MEM_CLKp
31 MEM_ADDR_CMD[30:0]
31 MEM_DQB[33:0]
31 MEM_DQSBp[3:0]
31 MEM_DQSBn[3:0]
31 MEM_DMBn[3:0]
31 MEM_DQ_ADDR_CMD[8:0]
31 MEM_DQS_ADDR_CMDp
31 MEM_DQS_ADDR_CMDn

R53 240 SODIMM_RZQ
R54 DNI SODIMM_REFCLKn
SODIMM_REFCLKp

U1D

MEM_DQ_ADDR_CMD8	CF43	IO, LVDS2B_25N, DQ20	
MEM_DQ_ADDR_CMD7	CH43	IO, LVDS2B_25P, DQ20	
MEM_DQ_ADDR_CMD6	CE42	IO, LVDS2B_26N, DQ20	
MEM_DQ_ADDR_CMD5	CG42	IO, LVDS2B_26P, DQ20	
	CF41	IO, LVDS2B_27N, DQ20	
MEM_DQ_ADDR_CMD4	CH41	IO, LVDS2B_27P, DQ20	
MEM_DQS_ADDR_CMDn	CE40	IO, LVDS2B_28N, DQSN20	
MEM_DQS_ADDR_CMDp	CG40	IO, LVDS2B_28P, DQS20	
MEM_DQ_ADDR_CMD3	CF39	IO, LVDS2B_29N, DQ20	
MEM_DQ_ADDR_CMD2	CH39	IO, LVDS2B_29P, DQ20	
MEM_DQ_ADDR_CMD1	CE38	IO, LVDS2B_30N, DQ20	
MEM_DQ_ADDR_CMD0	CG38	IO, LVDS2B_30P, DQ20	
MEM_ADDR_CMD30	CK43	IO, LVDS2B_31N, DQ21	
MEM_ADDR_CMD29	CM43	IO, LVDS2B_31P, DQ21	
MEM_ADDR_CMD28	CL42	IO, LVDS2B_32N, DQ21	
MEM_ADDR_CMD27	CN42	IO, LVDS2B_32P, DQ21	
MEM_ADDR_CMD26	CK41	IO, LVDS2B_33N, DQ21	
MEM_ADDR_CMD25	CM41	IO, LVDS2B_33P, DQ21	
MEM_ADDR_CMD24	CL40	IO, PLL_2B_B_CLKOUT1N, LVDS2B_34N, DQSN21	
MEM_ADDR_CMD23	CN40	IO, PLL_2B_B_CLKOUT1P, PLL_2B_B_CLKOUT1, PLL_2B_B_FB1, LVDS2B_34P, DQS21	
MEM_ADDR_CMD22	CK39	IO, LVDS2B_35N, DQ21	
SODIMM_RZQ	CM39	IO, RZQ_B_2B, LVDS2B_35P, DQ21	
SODIMM_REFCLKn	CL38	IO, CLK_B_2B_1N, LVDS2B_36N, DQ21	
SODIMM_REFCLKp	CN38	IO, CLK_B_2B_1P, LVDS2B_36P, DQ21	
MEM_ADDR_CMD21	CE36	IO, CLK_B_2B_0N, LVDS2B_37N, DQ22	
MEM_ADDR_CMD20	CG36	IO, CLK_B_2B_0P, LVDS2B_37P, DQ22	
MEM_ADDR_CMD19	CF35	IO, LVDS2B_38N, DQ22	
MEM_ADDR_CMD18	CH35	IO, LVDS2B_38P, DQ22	
MEM_ADDR_CMD17	CE34	IO, PLL_2B_B_CLKOUT0N, LVDS2B_39N, DQ22	
MEM_ADDR_CMD16	CG34	IO, PLL_2B_B_CLKOUT0P, PLL_2B_B_CLKOUT0, PLL_2B_B_FB0, LVDS2B_39P, DQ22	
MEM_ADDR_CMD15	CF33	IO, LVDS2B_40N, DQSN22	
MEM_ADDR_CMD14	CH33	IO, LVDS2B_40P, DQS22	
MEM_ADDR_CMD13	CE32	IO, LVDS2B_41N, DQ22	
MEM_ADDR_CMD12	CG32	IO, LVDS2B_41P, DQ22	
MEM_ADDR_CMD11	CF31	IO, LVDS2B_42N, DQ22	
MEM_ADDR_CMD10	CH31	IO, LVDS2B_42P, DQ22	
MEM_ADDR_CMD9	CL36	IO, LVDS2B_43N, DQ23	
MEM_ADDR_CMD8	CN36	IO, LVDS2B_43P, DQ23	
MEM_CLKn	CK35	IO, LVDS2B_44N, DQ23	
MEM_CLKp	CM35	IO, LVDS2B_44P, DQ23	
MEM_ADDR_CMD7	CL34	IO, LVDS2B_45N, DQ23	
MEM_ADDR_CMD6	CN34	IO, LVDS2B_45P, DQ23	
MEM_ADDR_CMD5	CK33	IO, LVDS2B_46N, DQSN23	
MEM_ADDR_CMD4	CM33	IO, LVDS2B_46P, DQS23	
MEM_ADDR_CMD3	CL32	IO, LVDS2B_47N, DQ23	
MEM_ADDR_CMD2	CN32	IO, LVDS2B_47P, DQ23	
MEM_ADDR_CMD1	CK31	IO, LVDS2B_48N, DQ23	
MEM_ADDR_CMD0	CM31	IO, LVDS2B_48P, DQ23	

BOT

		IO, LVDS2B_1N, DQ16	CT43 MEM_DQB5
		IO, LVDS2B_1P, DQ16	CV43 MEM_DQB1
		IO, LVDS2B_2N, DQ16	CR42 MEM_DQB4
		IO, LVDS2B_2P, DQ16	CU42 MEM_DQB0
		IO, LVDS2B_3N, DQ16	CT41
		IO, LVDS2B_3P, DQ16	CV41 MEM_DMBn0
		IO, LVDS2B_4N, DQSN16	CR40 MEM_DQSBn0
		IO, LVDS2B_4P, DQS16	CU40 MEM_DQSBp0
		IO, LVDS2B_5N, DQ16	CT39 MEM_DQB2
		IO, LVDS2B_5P, DQ16	CV39 MEM_DQB6
		IO, LVDS2B_6N, DQ16	CR38 MEM_DQB3
		IO, LVDS2B_6P, DQ16	CU38 MEM_DQB7
		IO, LVDS2B_7N, DQ17	CY43 MEM_DQB13
		IO, LVDS2B_7P, DQ17	DB43 MEM_DQB12
		IO, LVDS2B_8N, DQ17	DA42 MEM_DQB8
		IO, LVDS2B_8P, DQ17	DC42 MEM_DQB9
		IO, LVDS2B_9N, DQ17	CY41 MEM_DQB32
		IO, LVDS2B_9P, DQ17	DB41 MEM_DMBn1
		IO, PLL_2B_T_CLKOUT1N, LVDS2B_10N, DQSN17	DA40 MEM_DQSBn1
		IO, PLL_2B_T_CLKOUT1P, PLL_2B_T_CLKOUT1, PLL_2B_T_FB1, LVDS2B_10P, DQS17	DC40 MEM_DQSBp1
		IO, LVDS2B_11N, DQ17	CY39 MEM_DQB14
		IO, RZQ_T_2B, LVDS2B_11P, DQ17	DB39 MEM_DQB10
		IO, CLK_T_2B_1N, LVDS2B_12N, DQ17	DA38 MEM_DQB15
		IO, CLK_T_2B_1P, LVDS2B_12P, DQ17	DC38 MEM_DQB11
		IO, CLK_T_2B_0N, LVDS2B_13N, DQ18	CR36 MEM_DQB20
		IO, CLK_T_2B_0P, LVDS2B_13P, DQ18	CU36 MEM_DQB19
		IO, LVDS2B_14N, DQ18	CT35 MEM_DQB21
		IO, LVDS2B_14P, DQ18	CV35 MEM_DQB16
		IO, PLL_2B_T_CLKOUT0N, LVDS2B_15N, DQ18	CR34
		IO, PLL_2B_T_CLKOUT0P, PLL_2B_T_CLKOUT0, PLL_2B_T_FB0, LVDS2B_15P, DQ18	CU34 MEM_DMBn2
		IO, LVDS2B_16N, DQSN18	CT33 MEM_DQSBn2
		IO, LVDS2B_16P, DQS18	CV33 MEM_DQSBp2
		IO, LVDS2B_17N, DQ18	CR32 MEM_DQB17
		IO, LVDS2B_17P, DQ18	CU32 MEM_DQB23
		IO, LVDS2B_18N, DQ18	CT31 MEM_DQB18
		IO, LVDS2B_18P, DQ18	CV31 MEM_DQB22
		IO, LVDS2B_19N, DQ19	DA36 MEM_DQB25
		IO, LVDS2B_19P, DQ19	DC36 MEM_DQB28
		IO, LVDS2B_20N, DQ19	CY35 MEM_DQB24
		IO, LVDS2B_20P, DQ19	DB35 MEM_DQB29
		IO, LVDS2B_21N, DQ19	DA34 MEM_DQB33
		IO, LVDS2B_21P, DQ19	DC34 MEM_DMBn3
		IO, LVDS2B_22N, DQSN19	CY33 MEM_DQSBn3
		IO, LVDS2B_22P, DQS19	DB33 MEM_DQSBp3
		IO, LVDS2B_23N, DQ19	DA32 MEM_DQB26
		IO, LVDS2B_23P, DQ19	DC32 MEM_DQB30
		IO, LVDS2B_24N, DQ19	CY31 MEM_DQB27
		IO, LVDS2B_24P, DQ19	DB31 MEM_DQB31

TOP

Bank 2B

AGFB014R24A

VCCIO_FPGA_1.2V

R55 10.0K
R56 10.0K SODIMM_REFCLKn
R57 10.0K SODIMM_REFCLKp
R58 10.0K

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FPGA Bank - 2A

31 MEM_DQA[33:0]
31 MEM_DMAn[3:0]
31 MEM_DQSAp[3:0]
31 MEM_DQSAn[3:0]

CLKCleaner_INSEL00 53
CLKCleaner_INSEL01 53
CLKCleaner_INSEL10 53
CLKCleaner_INSEL11 53

CLKCleaner_GPIO0 53
CLKCleaner_GPIO1 53
CLKCleaner_GPIO2 53
CLKCleaner_GPIO3 53
CLKCleaner_GPIO4 53
CLKCleaner_GPIO5 53
CLKCleaner_GPIO6 53

CLKCleaner_status0 53
CLKCleaner_status1 53

CLKCleaner_SCL 53
CLKCleaner_SDA 53

ETH_RSTn 40
ETH_INTn 40
ETH_MDC 40
ETH_MDIO 40

referenceclk_1 53
referenceclk_2 53

SODIMM_I2C_SCL 31
SODIMM_I2C_SDA 31

U1E

CLKCleaner_GPIO1	CF57	IO, LVDS2A_25N, DQ28	IO, LVDS2A_1N, DQ24	CT57	MEM_DQA7
CLKCleaner_GPIO2	CH57	IO, LVDS2A_25P, DQ28	IO, LVDS2A_1P, DQ24	CV57	MEM_DQA3
CLKCleaner_GPIO3	CE56	IO, LVDS2A_26N, DQ28	IO, LVDS2A_2N, DQ24	CR56	MEM_DQA6
CLKCleaner_GPIO4	CG56	IO, LVDS2A_26P, DQ28	IO, LVDS2A_2P, DQ24	CU56	MEM_DQA2
CLKCleaner_GPIO5	CF55	IO, LVDS2A_27N, DQ28	IO, LVDS2A_3N, DQ24	CT55	
CLKCleaner_GPIO6	CH55	IO, LVDS2A_27P, DQ28	IO, LVDS2A_3P, DQ24	CV55	MEM_DMAn0
CLKCleaner_status0	CE54	IO, LVDS2A_28N, DQSN28	IO, LVDS2A_4N, DQSN24	CR54	MEM_DQSAn0
CLKCleaner_status1	CG54	IO, LVDS2A_28P, DQS28	IO, LVDS2A_4P, DQS24	CU54	MEM_DQSAp0
CLKCleaner_GPIO0	CF53	IO, LVDS2A_29N, DQ28	IO, LVDS2A_5N, DQ24	CT53	MEM_DQA5
	CH53	IO, LVDS2A_29P, DQ28	IO, LVDS2A_5P, DQ24	CV53	MEM_DQA1
CLKCleaner_INSEL00	CE52	IO, LVDS2A_30N, DQ28	IO, LVDS2A_6N, DQ24	CR52	MEM_DQA0
CLKCleaner_INSEL01	CG52	IO, LVDS2A_30P, DQ28	IO, LVDS2A_6P, DQ24	CU52	MEM_DQA4
CLKCleaner_INSEL10	CK57	IO, LVDS2A_31N, DQ29	IO, LVDS2A_7N, DQ25	CY57	MEM_DQA12
CLKCleaner_INSEL11	CM57	IO, LVDS2A_31P, DQ29	IO, LVDS2A_7P, DQ25	DB57	MEM_DQA13
ETH_RSTn	CL56	IO, LVDS2A_32N, DQ29	IO, LVDS2A_8N, DQ25	DA56	MEM_DQA8
ETH_INTn	CN56	IO, LVDS2A_32P, DQ29	IO, LVDS2A_8P, DQ25	DC56	MEM_DQA9
CLKCleaner_SCL	CK55	IO, LVDS2A_33N, DQ29	IO, LVDS2A_9N, DQ25	CY55	MEM_DQA32
	CM55	IO, LVDS2A_33P, DQ29	IO, LVDS2A_9P, DQ25	DB55	MEM_DMAn1
	CL54	IO, PLL_2A_B_CLKOUT1N, LVDS2A_34N, DQSN29	IO, PLL_2A_T_CLKOUT1N, LVDS2A_10N, DQSN25	DA54	MEM_DQSAn1
	CN54	IO, PLL_2A_B_CLKOUT1P, PLL_2A_B_CLKOUT1, PLL_2A_B_FB1, LVDS2A_34P, DQS29	IO, PLL_2A_T_CLKOUT1P, PLL_2A_T_CLKOUT1, PLL_2A_T_FB1, LVDS2A_10P, DQS25	DC54	MEM_DQSAp1
	CK53	IO, LVDS2A_35N, DQ29	IO, LVDS2A_11N, DQ25	CY53	MEM_DQA14
	CM53	IO, RZQ_B_2A, LVDS2A_35P, DQ29	IO, RZQ_T_2A, LVDS2A_11P, DQ25	DB53	MEM_DQA15
	CL52	IO, CLK_B_2A_1N, LVDS2A_36N, DQ29	IO, CLK_T_2A_1N, LVDS2A_12N, DQ25	DA52	MEM_DQA10
	CN52	IO, CLK_B_2A_1P, LVDS2A_36P, DQ29	IO, CLK_T_2A_1P, LVDS2A_12P, DQ25	DC52	MEM_DQA11
	CE50	IO, CLK_B_2A_0N, LVDS2A_37N, DQ30	IO, CLK_T_2A_0N, LVDS2A_13N, DQ26	CR50	MEM_DQA22
	CG50	IO, CLK_B_2A_0P, LVDS2A_37P, DQ30	IO, CLK_T_2A_0P, LVDS2A_13P, DQ26	CU50	MEM_DQA19
	CF49	IO, LVDS2A_38N, DQ30	IO, LVDS2A_14N, DQ26	CT49	MEM_DQA18
	CH49	IO, LVDS2A_38P, DQ30	IO, LVDS2A_14P, DQ26	CV49	MEM_DQA23
CLKCleaner_SDA	CE48	IO, PLL_2A_B_CLKOUT0N, LVDS2A_39N, DQ30	IO, PLL_2A_T_CLKOUT0N, LVDS2A_15N, DQ26	CR48	
	CG48	IO, PLL_2A_B_CLKOUT0P, PLL_2A_B_CLKOUT0, PLL_2A_B_FB0, LVDS2A_39P, DQ30	IO, PLL_2A_T_CLKOUT0P, PLL_2A_T_CLKOUT0, PLL_2A_T_FB0, LVDS2A_15P, DQ26	CU48	MEM_DMAn2
	CF47	IO, LVDS2A_40N, DQSN30	IO, LVDS2A_16N, DQSN26	CT47	MEM_DQSAn2
	CH47	IO, LVDS2A_40P, DQS30	IO, LVDS2A_16P, DQS26	CV47	MEM_DQSAp2
ETH_MDIO	CE46	IO, LVDS2A_41N, DQ30	IO, LVDS2A_17N, DQ26	CR46	MEM_DQA17
	CG46	IO, LVDS2A_41P, DQ30	IO, LVDS2A_17P, DQ26	CU46	MEM_DQA21
	CF45	IO, LVDS2A_42N, DQ30	IO, LVDS2A_18N, DQ26	CT45	MEM_DQA16
	CH45	IO, LVDS2A_42P, DQ30	IO, LVDS2A_18P, DQ26	CV45	MEM_DQA20
ETH_MDC	CL50	IO, LVDS2A_43N, DQ31	IO, LVDS2A_19N, DQ27	DA50	MEM_DQA28
	CN50	IO, LVDS2A_43P, DQ31	IO, LVDS2A_19P, DQ27	DC50	MEM_DQA29
	CK49	IO, LVDS2A_44N, DQ31	IO, LVDS2A_20N, DQ27	CY49	MEM_DQA30
	CM49	IO, LVDS2A_44P, DQ31	IO, LVDS2A_20P, DQ27	DB49	MEM_DQA25
SODIMM_I2C_SDA	CL48	IO, LVDS2A_45N, DQ31	IO, LVDS2A_21N, DQ27	DA48	MEM_DQA33
	CN48	IO, LVDS2A_45P, DQ31	IO, LVDS2A_21P, DQ27	DC48	MEM_DMAn3
	CK47	IO, LVDS2A_46N, DQSN31	IO, LVDS2A_22N, DQSN27	CY47	MEM_DQSAn3
	CM47	IO, LVDS2A_46P, DQS31	IO, LVDS2A_22P, DQS27	DB47	MEM_DQSAp3
SODIMM_I2C_SCL	CL46	IO, LVDS2A_47N, DQ31	IO, LVDS2A_23N, DQ27	DA46	MEM_DQA24
	CN46	IO, LVDS2A_47P, DQ31	IO, LVDS2A_23P, DQ27	DC46	MEM_DQA31
	CK45	IO, LVDS2A_48N, DQ31	IO, LVDS2A_24N, DQ27	CY45	MEM_DQA26
	CM45	IO, LVDS2A_48P, DQ31	IO, LVDS2A_24P, DQ27	DB45	MEM_DQA27

BOT TOP

Bank 2A

AGFB014R24A

3.3V
VCCIO_FPGA_1.8V
R59 DNI
R61 DNI
referenceclk_1 R940 0
R60 51
referenceclk_2 R1025 0
R62 120

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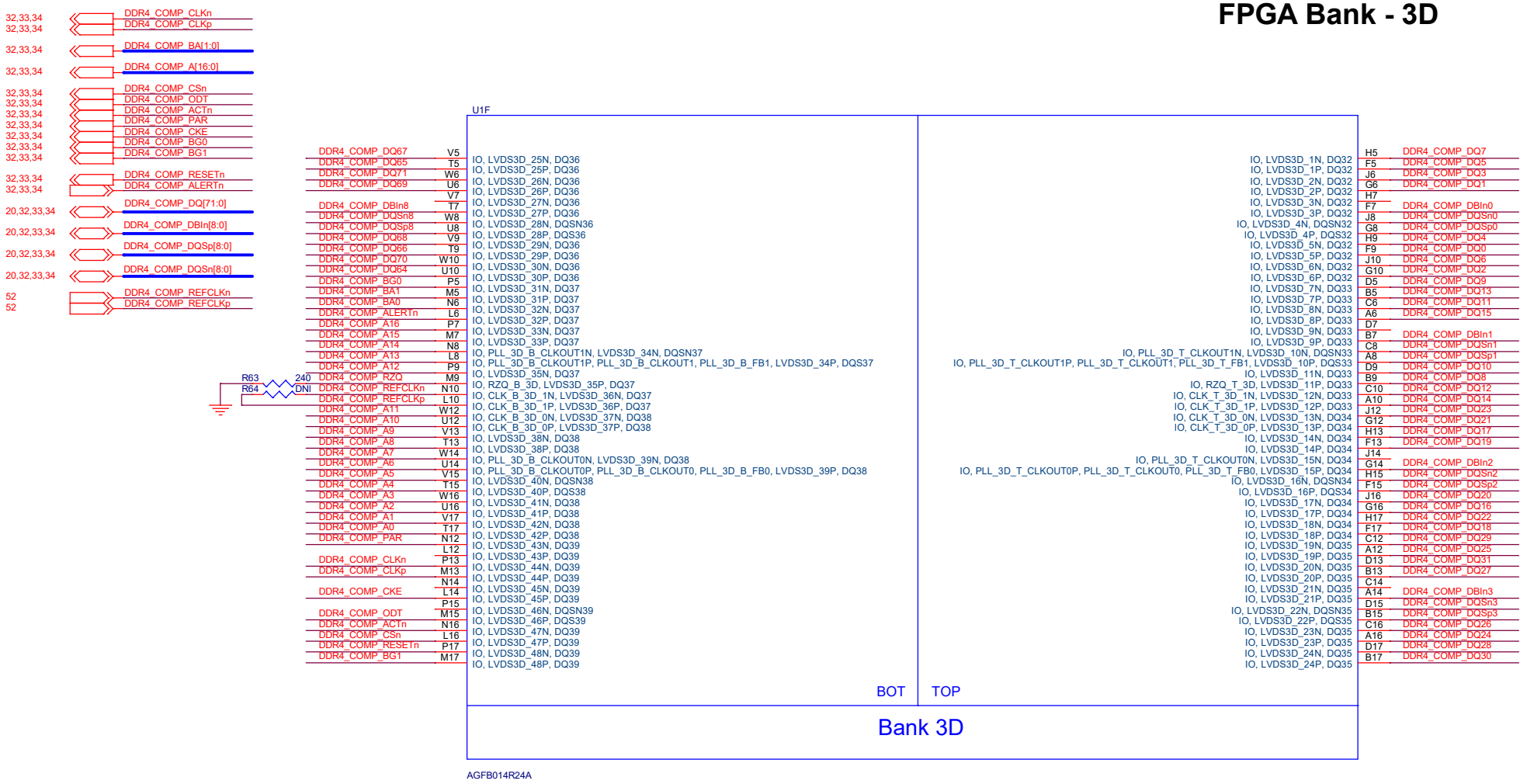
FPGA Bank - 3D



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FPGA Bank - 3C

19,32,33,34 DDR4_COMP_DQ[71:0]
19,32,33,34 DDR4_COMP_DBIn[8:0]
19,32,33,34 DDR4_COMP_DQSp[8:0]
19,32,33,34 DDR4_COMP_DQSn[8:0]

U1G

DDR4_COMP_DQ35	V19	IO, LVDS3C_25N, DQ44	
DDR4_COMP_DQ37	T19	IO, LVDS3C_25P, DQ44	
DDR4_COMP_DQ39	W20	IO, LVDS3C_26N, DQ44	
DDR4_COMP_DQ33	U20	IO, LVDS3C_26P, DQ44	
	V21	IO, LVDS3C_27N, DQ44	
DDR4_COMP_DBIn4	T21	IO, LVDS3C_27P, DQ44	
DDR4_COMP_DQSn4	W22	IO, LVDS3C_28N, DQSN44	
DDR4_COMP_DQSp4	U22	IO, LVDS3C_28P, DQS44	
DDR4_COMP_DQ36	V23	IO, LVDS3C_29N, DQ44	
DDR4_COMP_DQ32	T23	IO, LVDS3C_29P, DQ44	
DDR4_COMP_DQ38	W24	IO, LVDS3C_30N, DQ44	
DDR4_COMP_DQ34	U24	IO, LVDS3C_30P, DQ44	
DDR4_COMP_DQ41	P19	IO, LVDS3C_31N, DQ45	
DDR4_COMP_DQ45	M19	IO, LVDS3C_31P, DQ45	
DDR4_COMP_DQ43	N20	IO, LVDS3C_32N, DQ45	
DDR4_COMP_DQ47	L20	IO, LVDS3C_32P, DQ45	
	P21	IO, LVDS3C_33N, DQ45	
DDR4_COMP_DBIn5	M21	IO, LVDS3C_33P, DQ45	
DDR4_COMP_DQSn5	N22	IO, PLL_3C_B_CLKOUT1N, LVDS3C_34N, DQSN45	
DDR4_COMP_DQSp5	L22	IO, PLL_3C_B_CLKOUT1P, PLL_3C_B_CLKOUT1, PLL_3C_B_FB1, LVDS3C_34P, DQS45	
DDR4_COMP_DQ40	P23	IO, LVDS3C_35N, DQ45	
DDR4_COMP_DQ42	M23	IO, RZQ_B_3C, LVDS3C_35P, DQ45	
DDR4_COMP_DQ46	N24	IO, CLK_B_3C_1N, LVDS3C_36N, DQ45	
DDR4_COMP_DQ44	L24	IO, CLK_B_3C_1P, LVDS3C_36P, DQ45	
DDR4_COMP_DQ51	W26	IO, CLK_B_3C_0N, LVDS3C_37N, DQ46	
DDR4_COMP_DQ53	U26	IO, CLK_B_3C_0P, LVDS3C_37P, DQ46	
DDR4_COMP_DQ55	V27	IO, LVDS3C_38N, DQ46	
DDR4_COMP_DQ49	T27	IO, LVDS3C_38P, DQ46	
	W28	IO, PLL_3C_B_CLKOUT0N, LVDS3C_39N, DQ46	
DDR4_COMP_DBIn6	U28	IO, PLL_3C_B_CLKOUT0P, PLL_3C_B_CLKOUT0, PLL_3C_B_FB0, LVDS3C_39P, DQ46	
DDR4_COMP_DQSn6	V29	IO, LVDS3C_40N, DQSN46	
DDR4_COMP_DQSp6	T29	IO, LVDS3C_40P, DQS46	
DDR4_COMP_DQ52	W30	IO, LVDS3C_41N, DQ46	
DDR4_COMP_DQ48	U30	IO, LVDS3C_41P, DQ46	
DDR4_COMP_DQ54	V31	IO, LVDS3C_42N, DQ46	
DDR4_COMP_DQ50	T31	IO, LVDS3C_42P, DQ46	
DDR4_COMP_DQ57	N26	IO, LVDS3C_43N, DQ47	
DDR4_COMP_DQ61	L26	IO, LVDS3C_43P, DQ47	
DDR4_COMP_DQ59	P27	IO, LVDS3C_44N, DQ47	
DDR4_COMP_DQ63	M27	IO, LVDS3C_44P, DQ47	
	N28	IO, LVDS3C_45N, DQ47	
DDR4_COMP_DBIn7	L28	IO, LVDS3C_45P, DQ47	
DDR4_COMP_DQSn7	P29	IO, LVDS3C_46N, DQSN47	
DDR4_COMP_DQSp7	M29	IO, LVDS3C_46P, DQS47	
DDR4_COMP_DQ58	N30	IO, LVDS3C_47N, DQ47	
DDR4_COMP_DQ56	L30	IO, LVDS3C_47P, DQ47	
DDR4_COMP_DQ60	P31	IO, LVDS3C_48N, DQ47	
DDR4_COMP_DQ62	M31	IO, LVDS3C_48P, DQ47	

		IO, LVDS3C_1N, DQ40	H19
		IO, LVDS3C_1P, DQ40	F19
		IO, LVDS3C_2N, DQ40	J20
		IO, LVDS3C_2P, DQ40	G20
		IO, LVDS3C_3N, DQ40	H21
		IO, LVDS3C_3P, DQ40	F21
		IO, LVDS3C_4N, DQSN40	J22
		IO, LVDS3C_4P, DQS40	G22
		IO, LVDS3C_5N, DQ40	H23
		IO, LVDS3C_5P, DQ40	F23
		IO, LVDS3C_6N, DQ40	J24
		IO, LVDS3C_6P, DQ40	G24
		IO, LVDS3C_7N, DQ41	D19
		IO, LVDS3C_7P, DQ41	B19
		IO, LVDS3C_8N, DQ41	C20
		IO, LVDS3C_8P, DQ41	A20
		IO, LVDS3C_9N, DQ41	D21
		IO, LVDS3C_9P, DQ41	B21
		IO, PLL_3C_T_CLKOUT1N, LVDS3C_10N, DQSN41	C22
		IO, PLL_3C_T_CLKOUT1P, PLL_3C_T_CLKOUT1, PLL_3C_T_FB1, LVDS3C_10P, DQS41	A22
		IO, LVDS3C_11N, DQ41	D23
		IO, RZQ_T_3C, LVDS3C_11P, DQ41	B23
		IO, CLK_T_3C_1N, LVDS3C_12N, DQ41	C24
		IO, CLK_T_3C_1P, LVDS3C_12P, DQ41	A24
		IO, CLK_T_3C_0N, LVDS3C_13N, DQ42	J26
		IO, CLK_T_3C_0P, LVDS3C_13P, DQ42	G26
		IO, LVDS3C_14N, DQ42	H27
		IO, LVDS3C_14P, DQ42	F27
		IO, PLL_3C_T_CLKOUT0N, LVDS3C_15N, DQ42	J28
		IO, PLL_3C_T_CLKOUT0P, PLL_3C_T_CLKOUT0, PLL_3C_T_FB0, LVDS3C_15P, DQ42	G28
		IO, LVDS3C_16N, DQSN42	H29
		IO, LVDS3C_16P, DQS42	F29
		IO, LVDS3C_17N, DQ42	J30
		IO, LVDS3C_17P, DQ42	G30
		IO, LVDS3C_18N, DQ42	H31
		IO, LVDS3C_18P, DQ42	F31
		IO, LVDS3C_19N, DQ43	C26
		IO, LVDS3C_19P, DQ43	A26
		IO, LVDS3C_20N, DQ43	D27
		IO, LVDS3C_20P, DQ43	B27
		IO, LVDS3C_21N, DQ43	C28
		IO, LVDS3C_21P, DQ43	A28
		IO, LVDS3C_22N, DQSN43	D29
		IO, LVDS3C_22P, DQS43	B29
		IO, LVDS3C_23N, DQ43	C30
		IO, LVDS3C_23P, DQ43	A30
		IO, LVDS3C_24N, DQ43	D31
		IO, LVDS3C_24P, DQ43	B31

BOT TOP

Bank 3C

AGFB014R24A

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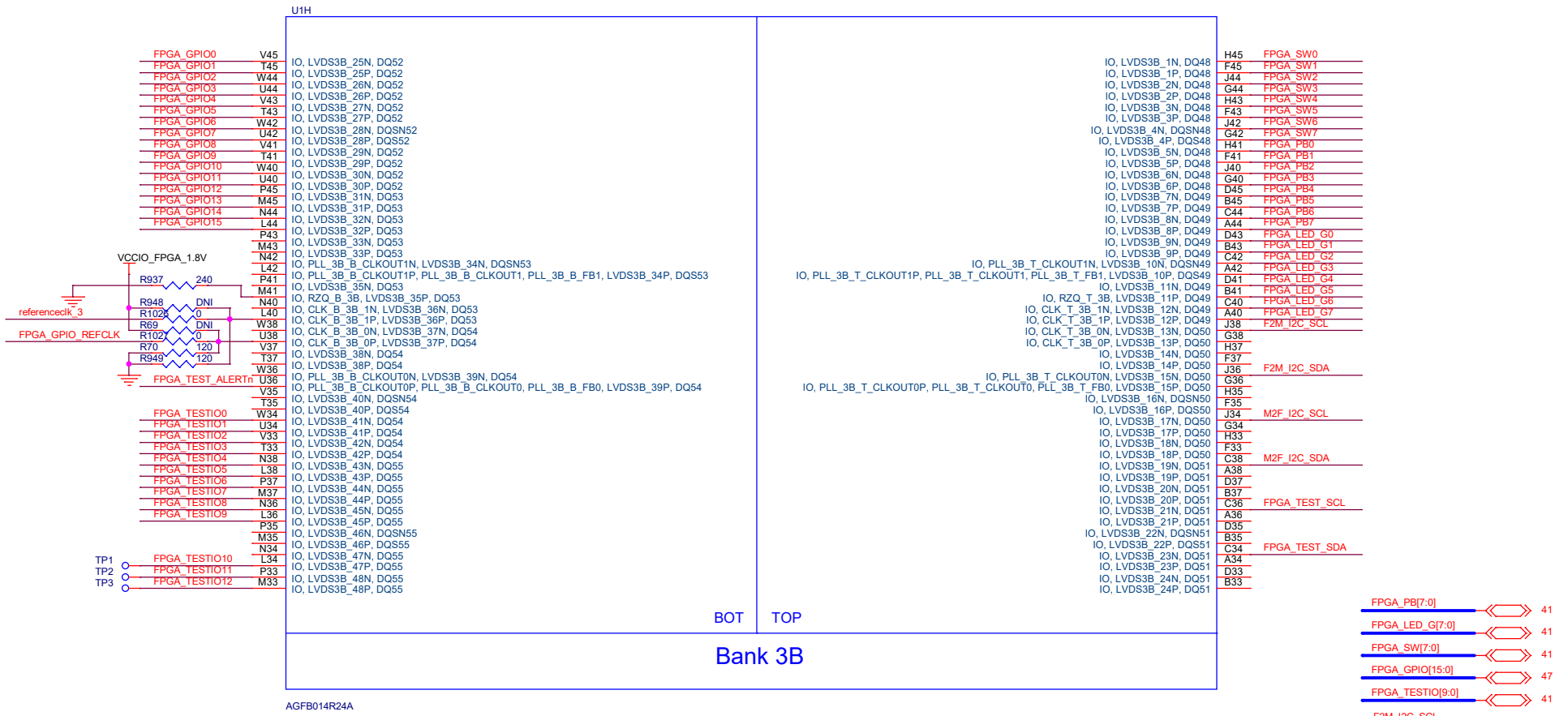
FPGA Bank - 3B



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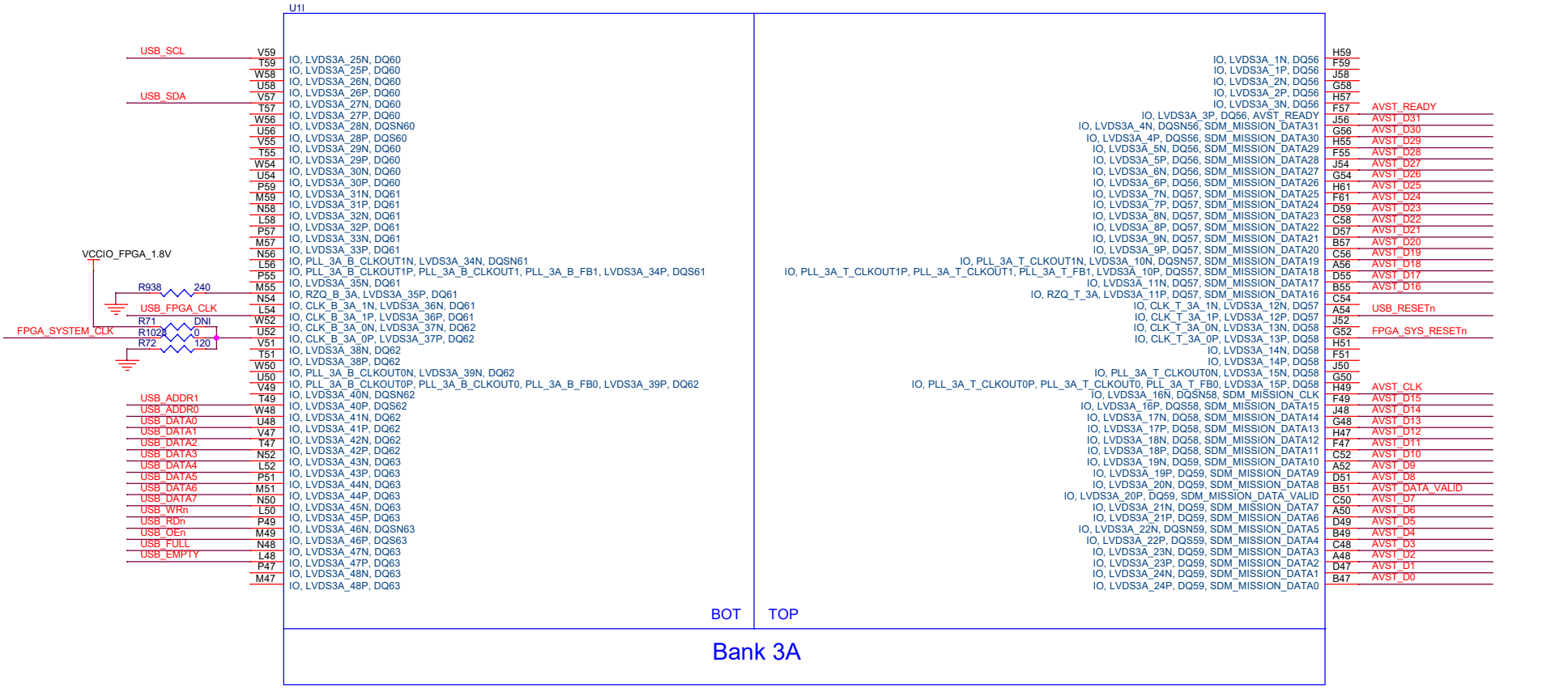
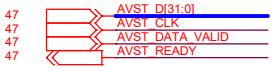
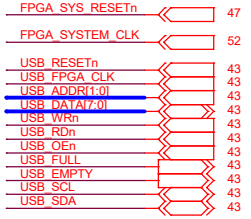
FPGA Bank - 3A







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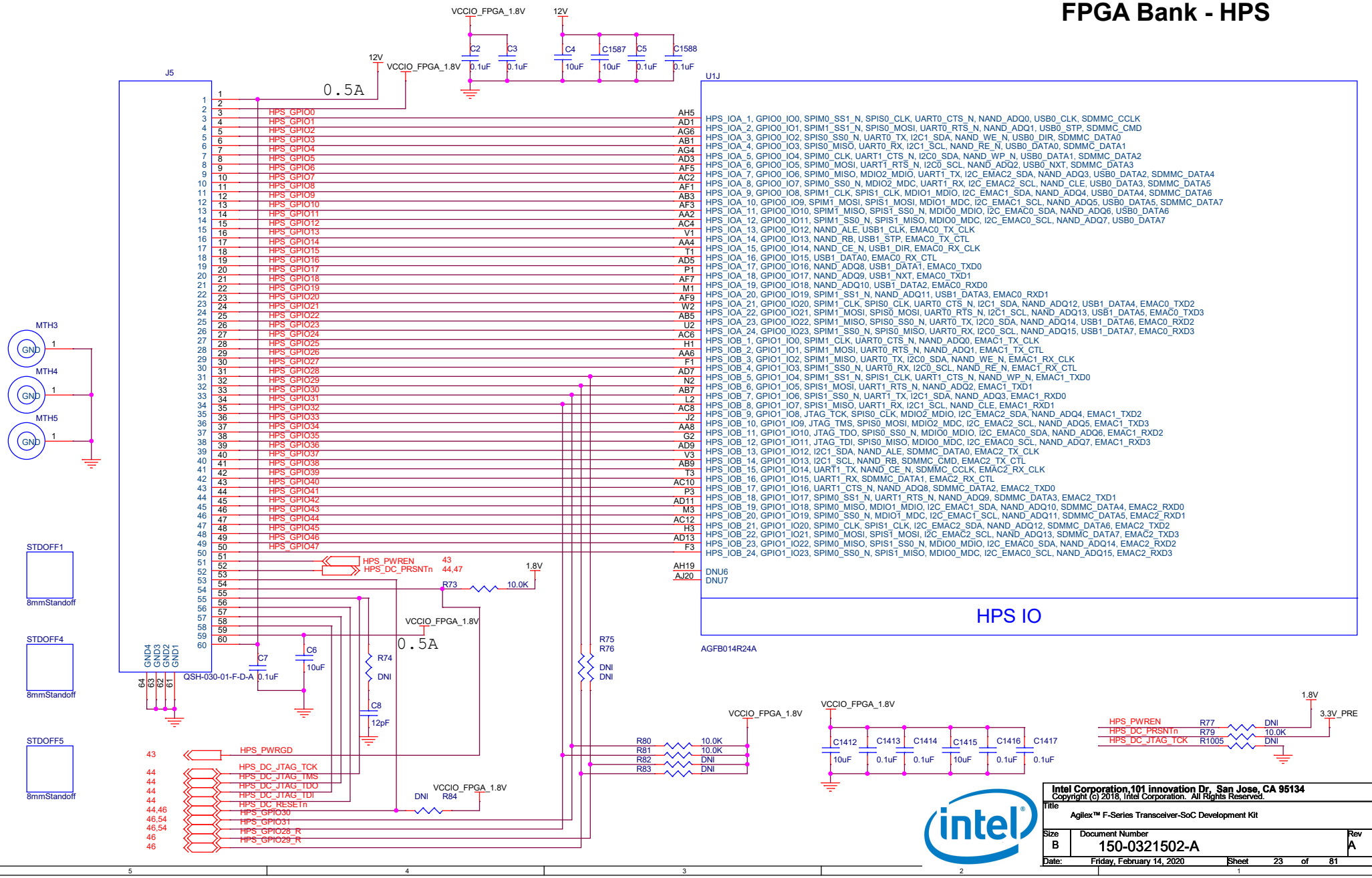
FPGA Bank - HPS



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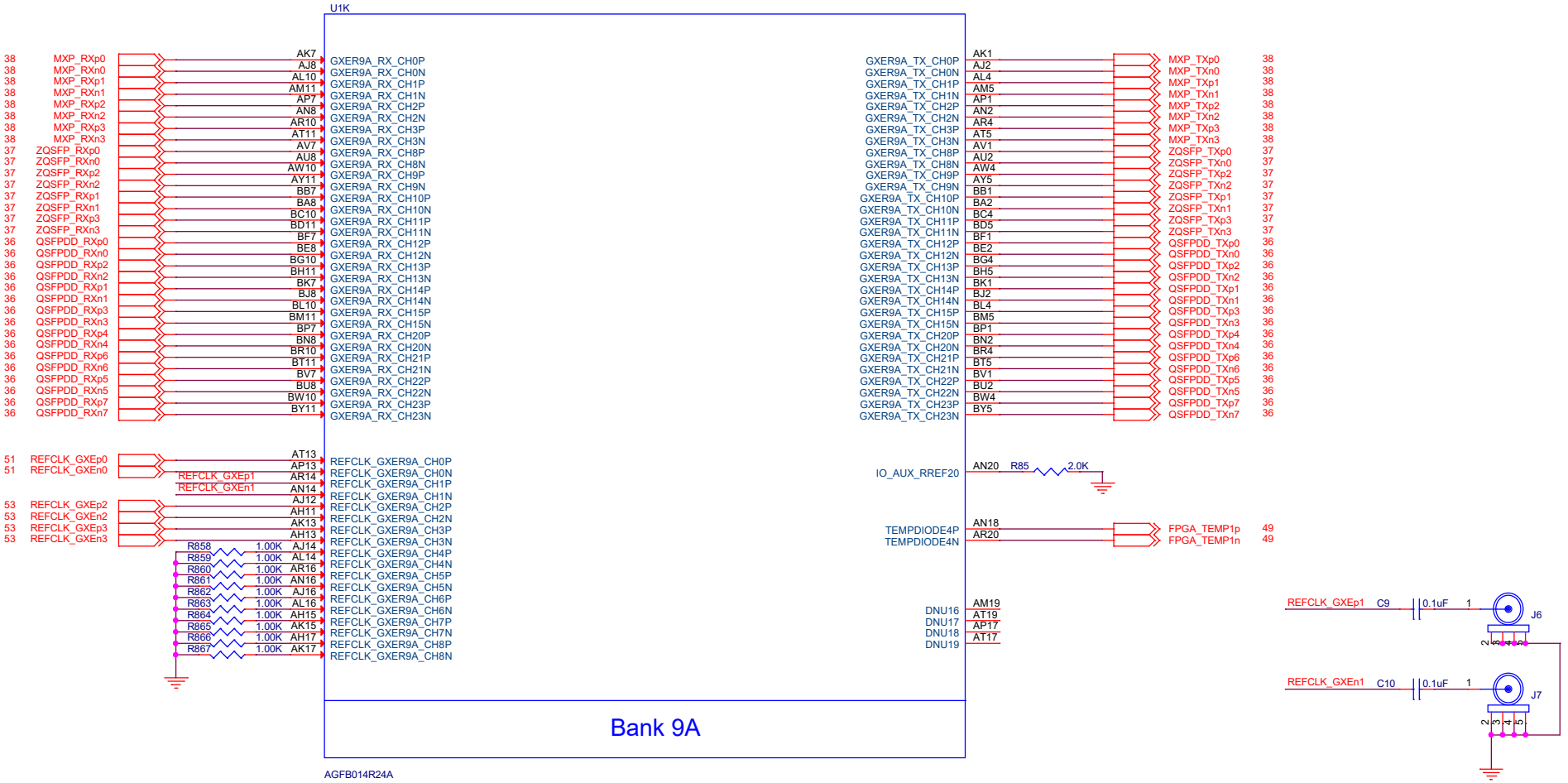
FPGA Bank - 9A E-tile



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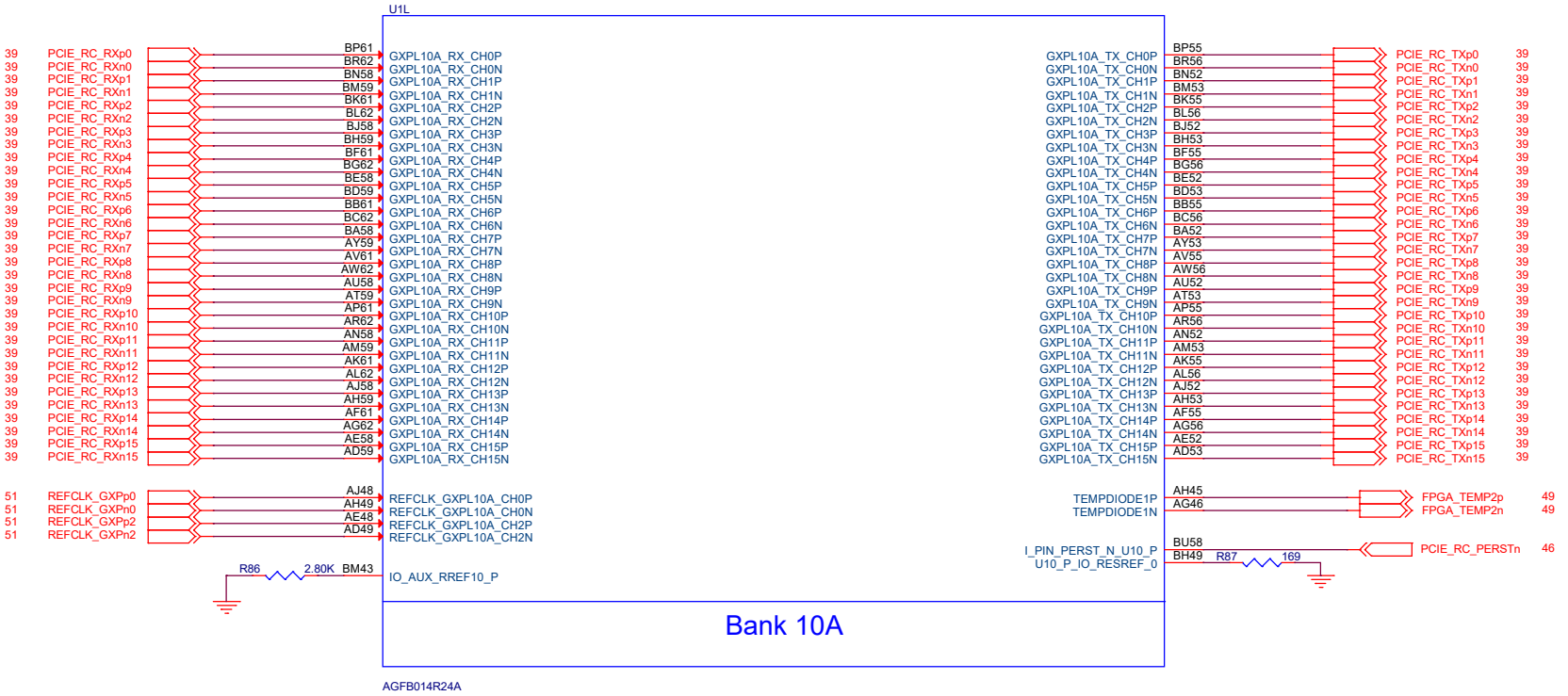
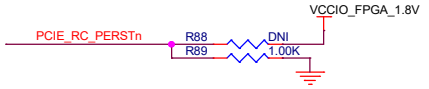
FPGA Bank - 10A P-tile





Different power group

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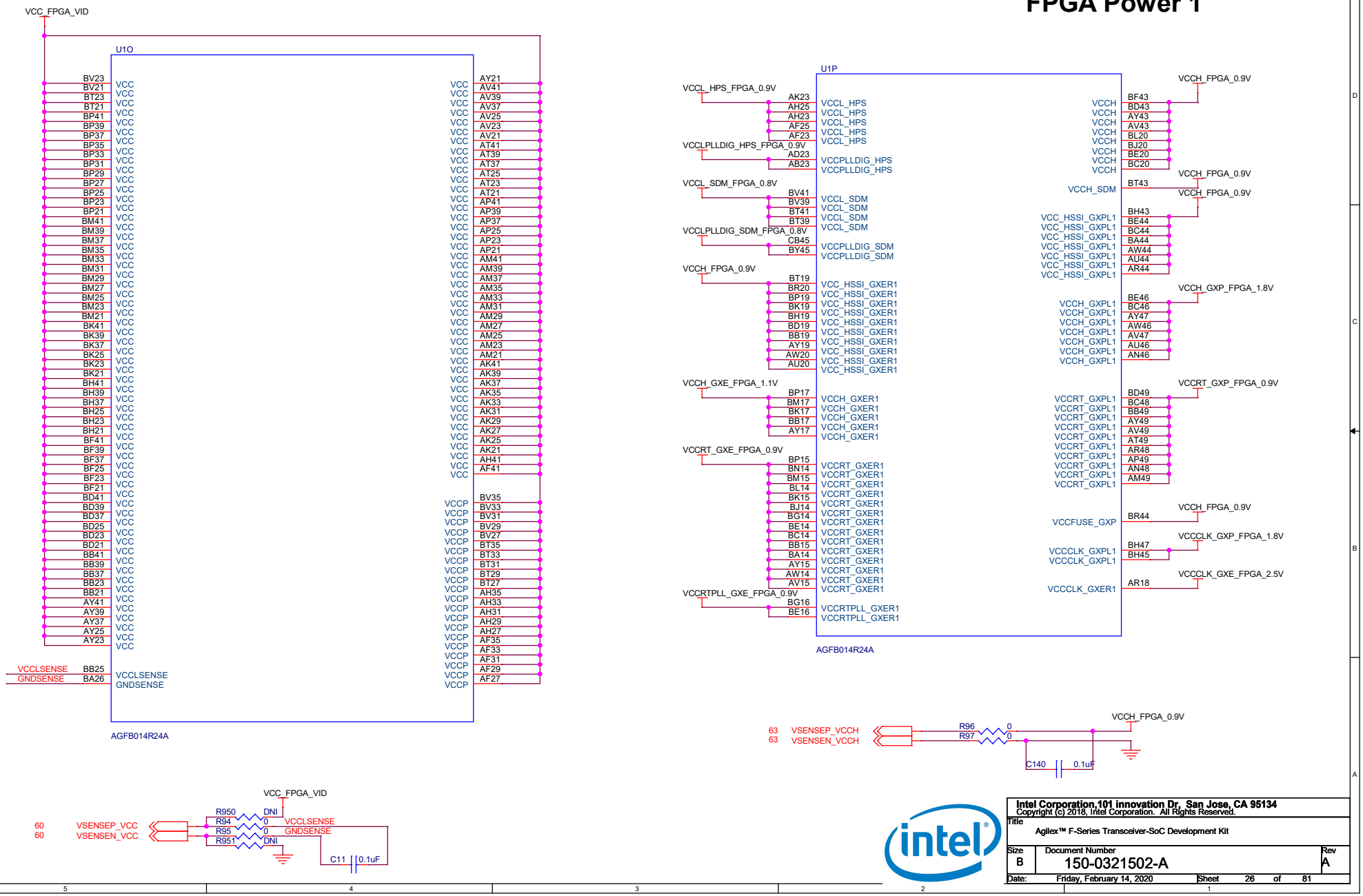
FPGA Power 1



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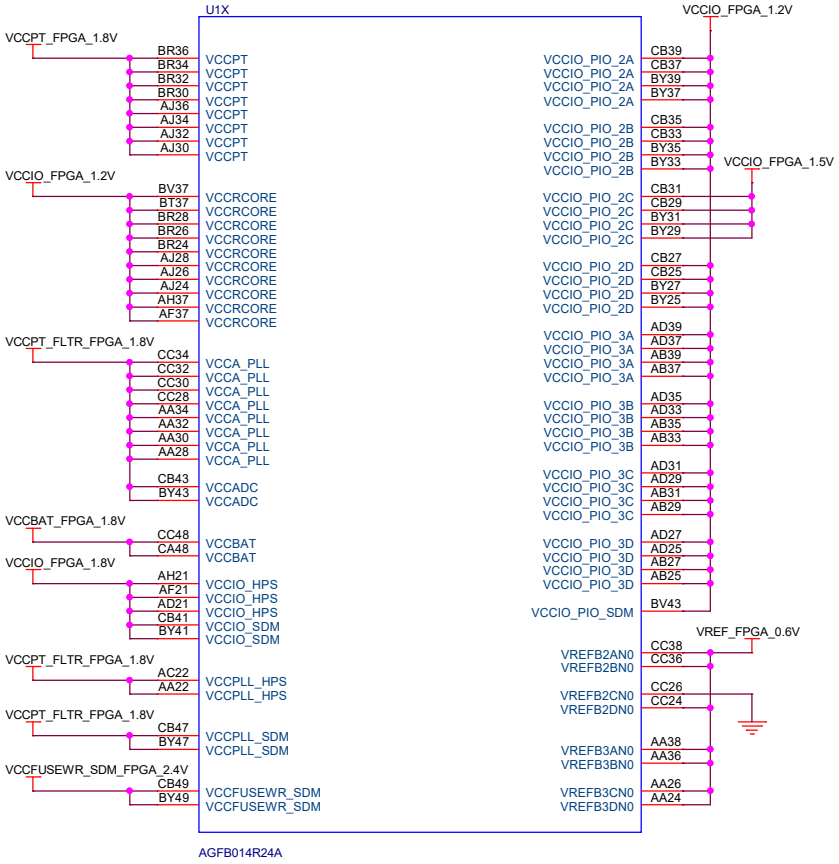
FPGA Power 2



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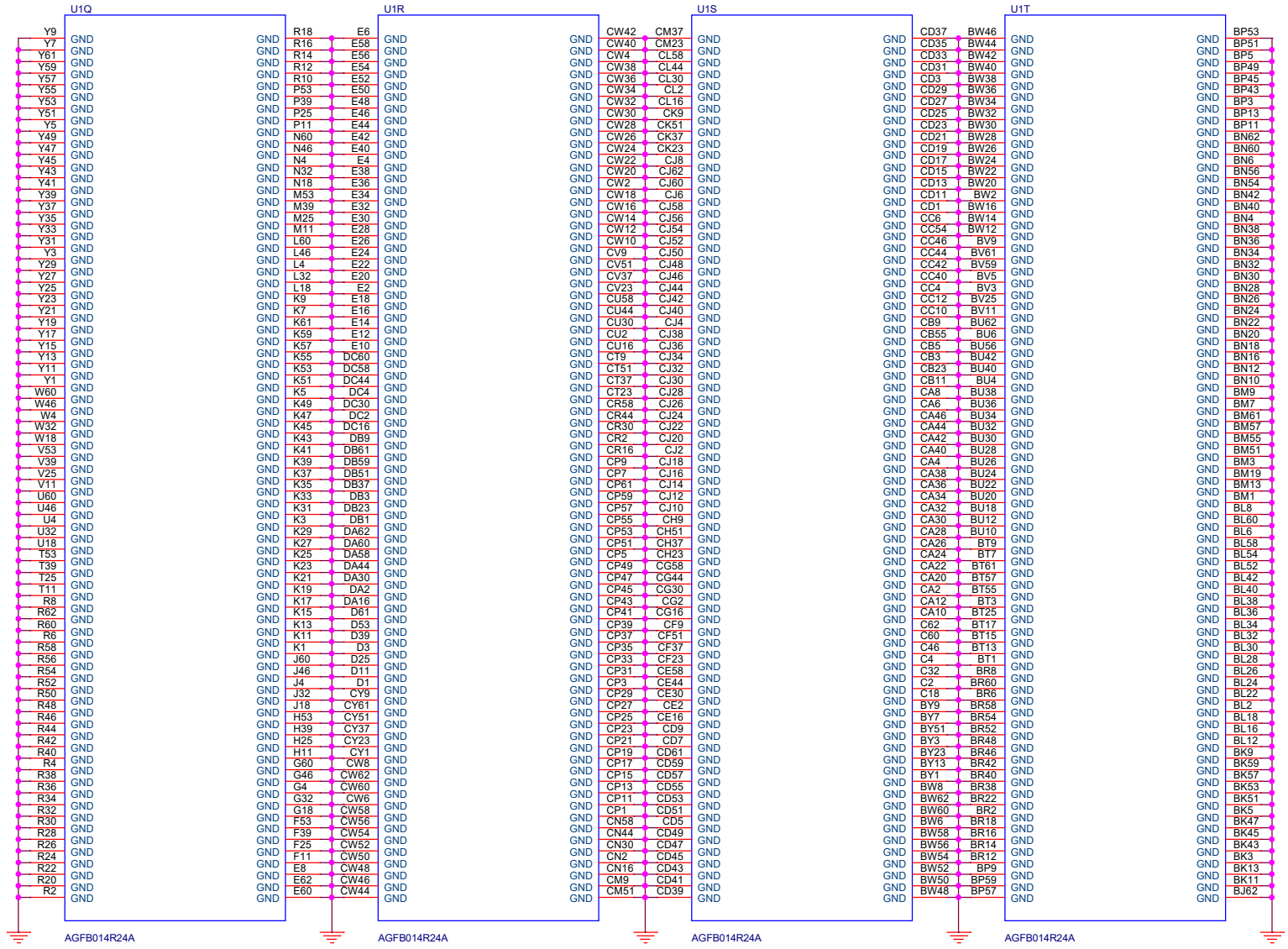
FPGA GND 1



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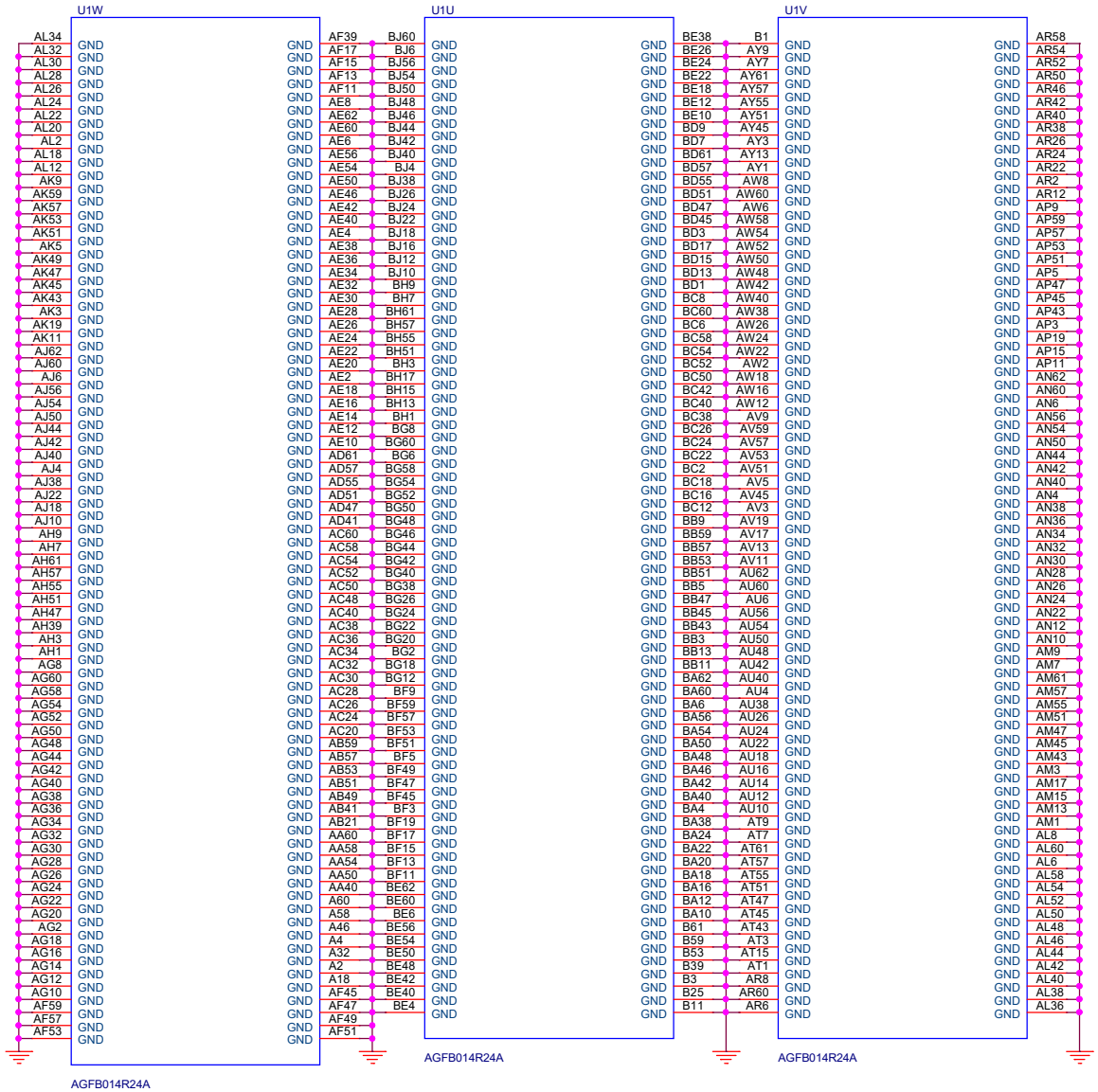
FPGA GND 2



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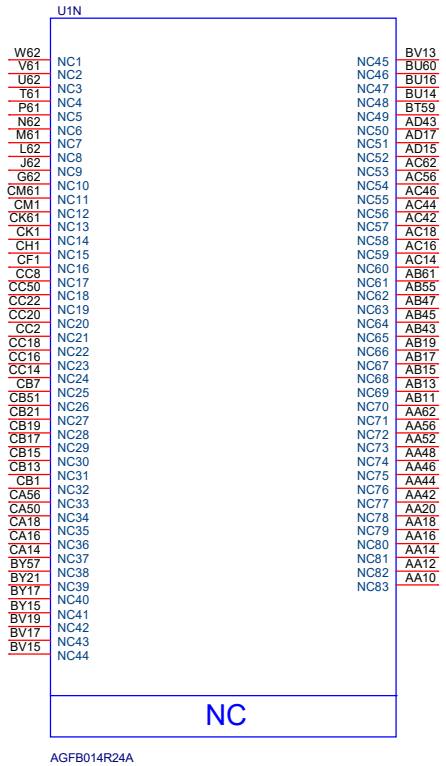
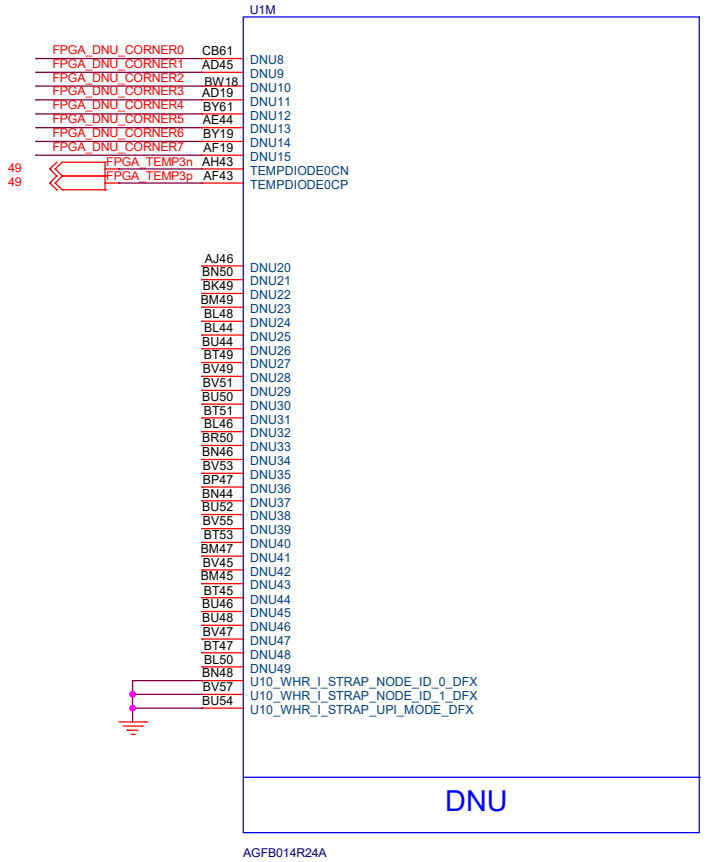
FPGA NC/DNU





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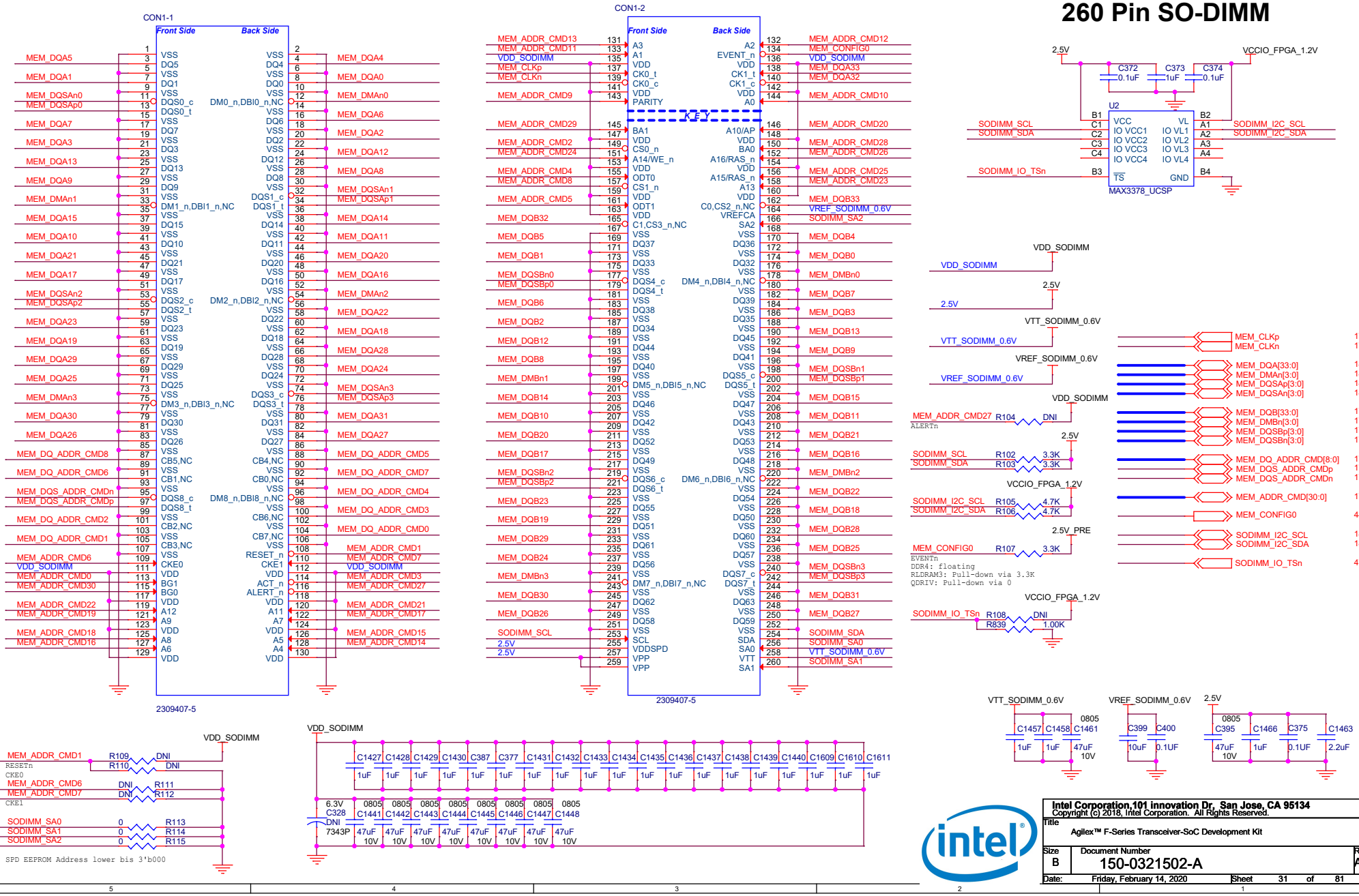
260 Pin SO-DIMM



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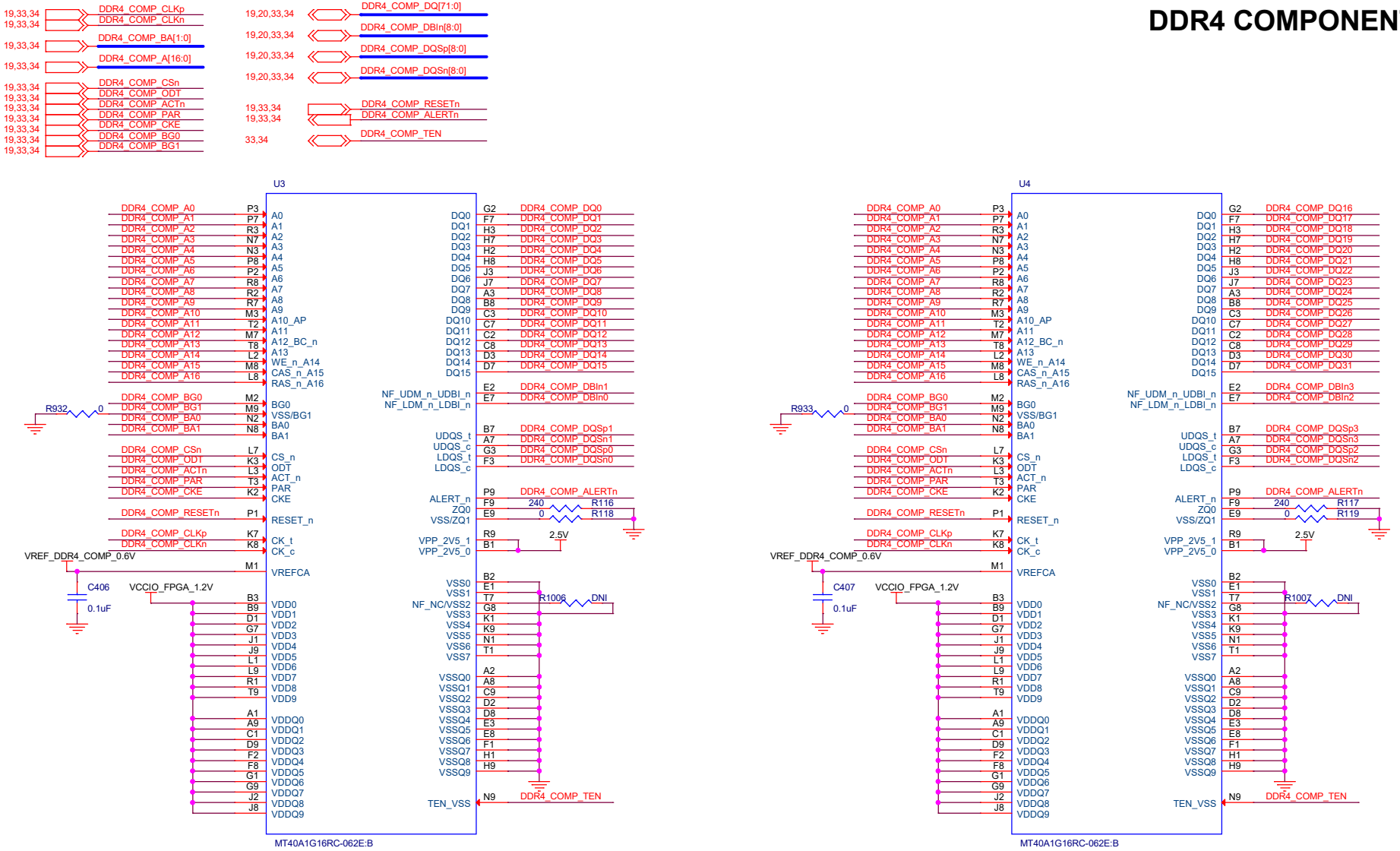
DDR4 COMPONENT #1/#2



16Gb, 0.625ns@CL=22 (DDR4-3200)

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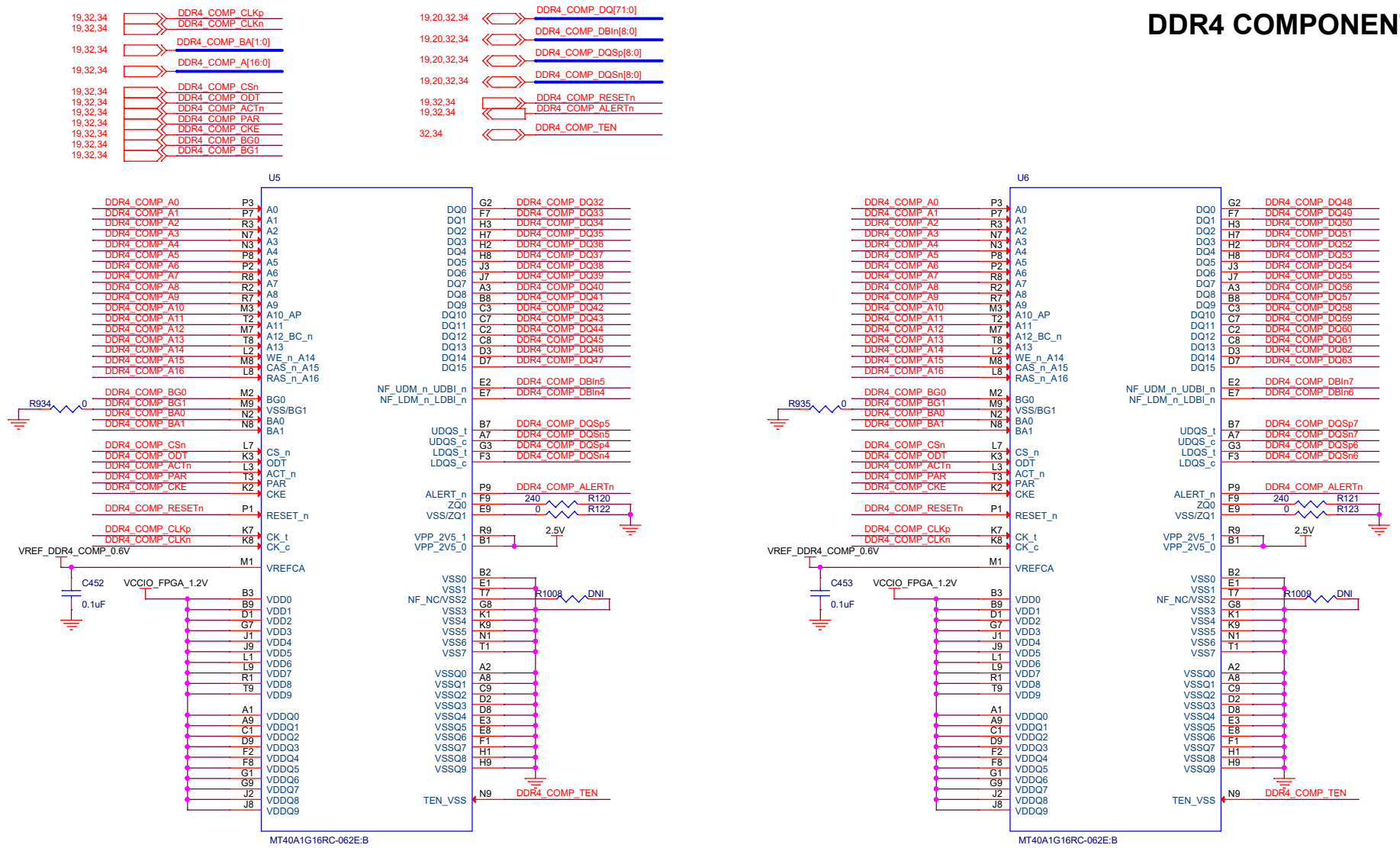
DDR4 COMPONENT #3/#4



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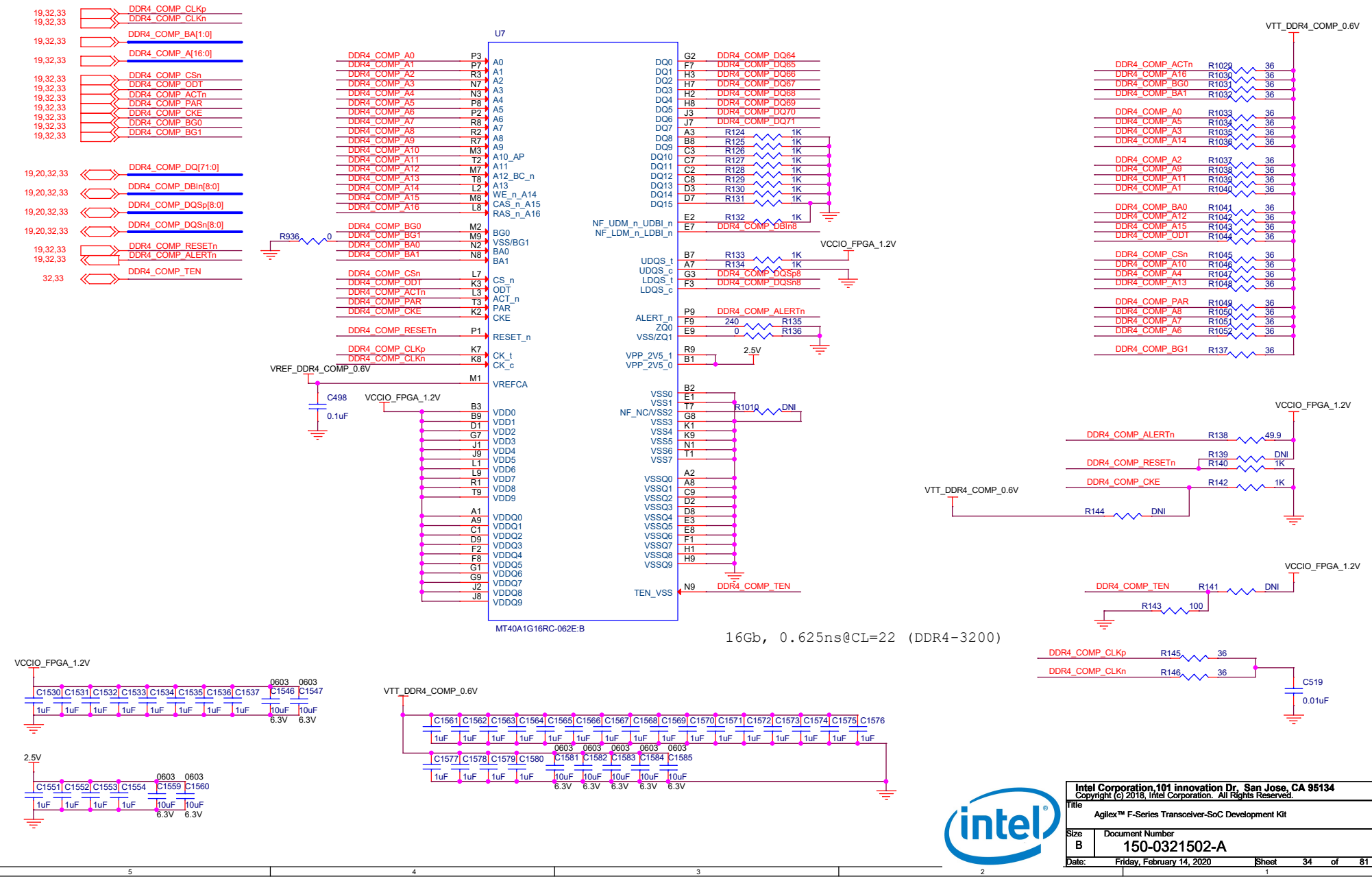
DDR4 COMPONENT #5 & Termination



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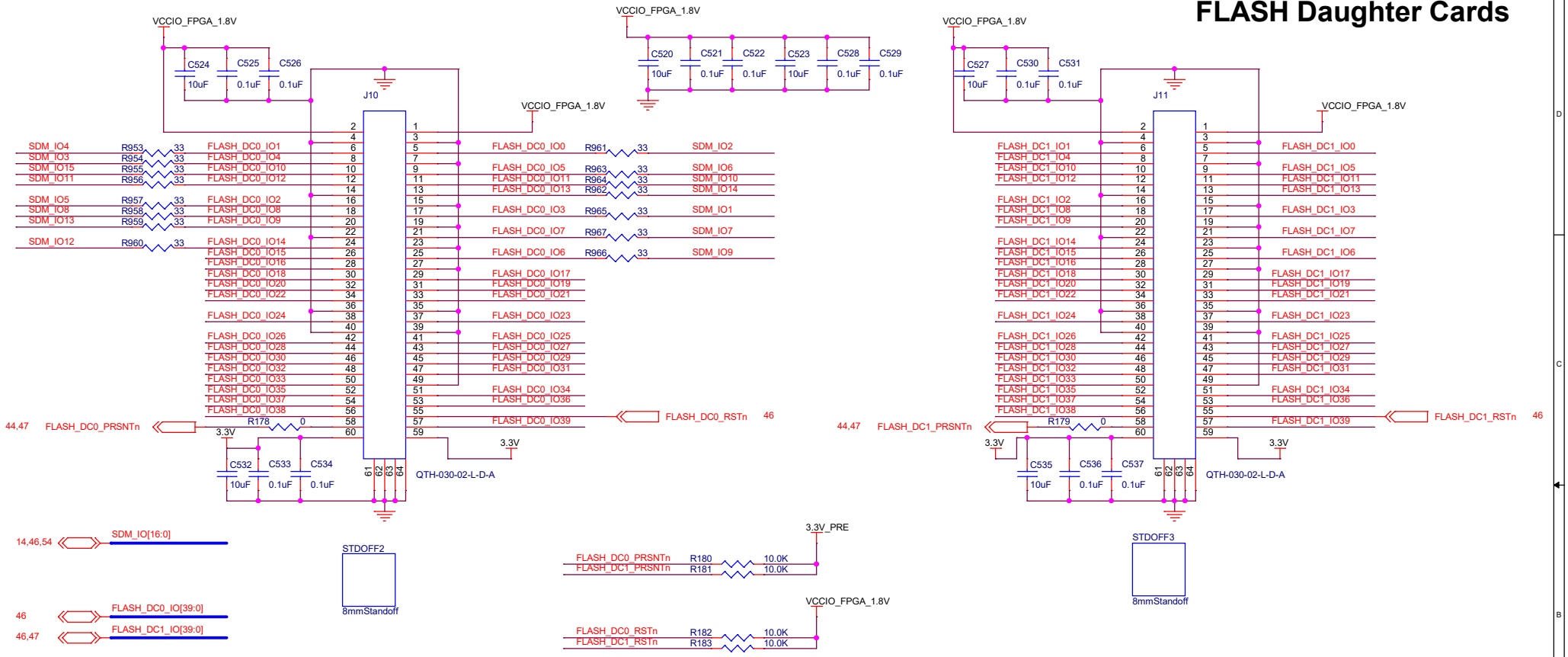
FLASH Daughter Cards



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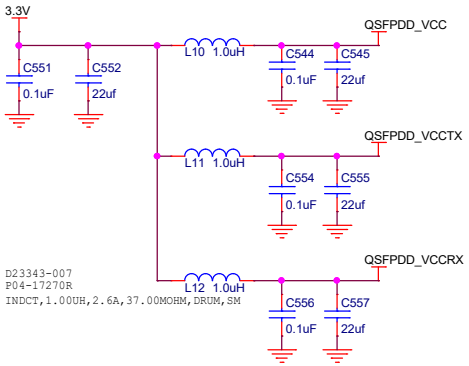
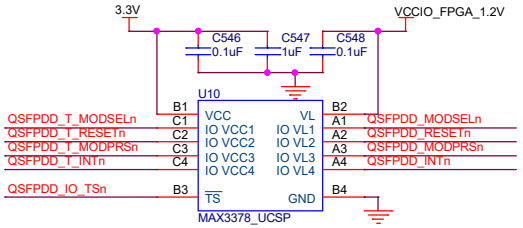
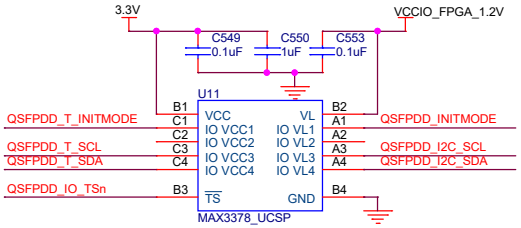
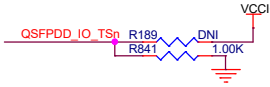
QSFPDD 1x1









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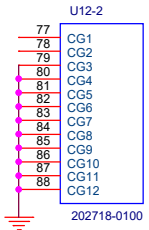
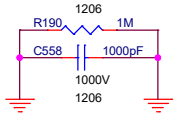
Molex/Fit-FoxCONN
CONN - 1x1 QSFP DD CAGE ASSEMBLY



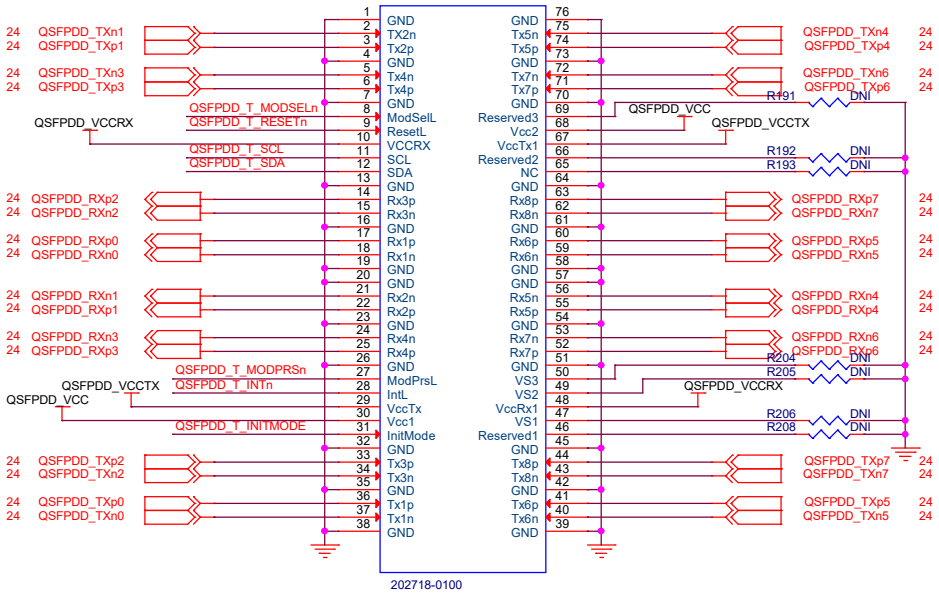
GND_QSFPDD_CAGE

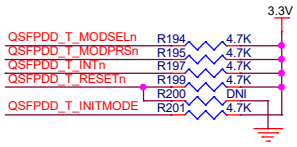


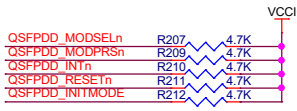
GND_QSFPDD_CAGE

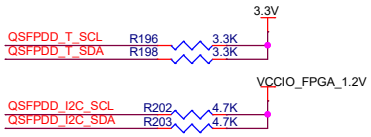
Cage GND on top layer

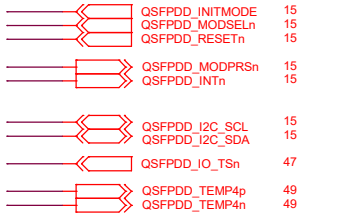
ModSelL: Module Select
ResetL: Module Reset
ModPrsL: Module Present
IntL: Interrupt
InitMode: Initialization mode (LPMODE)

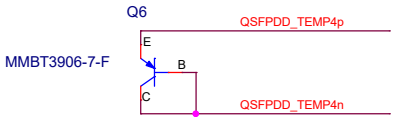












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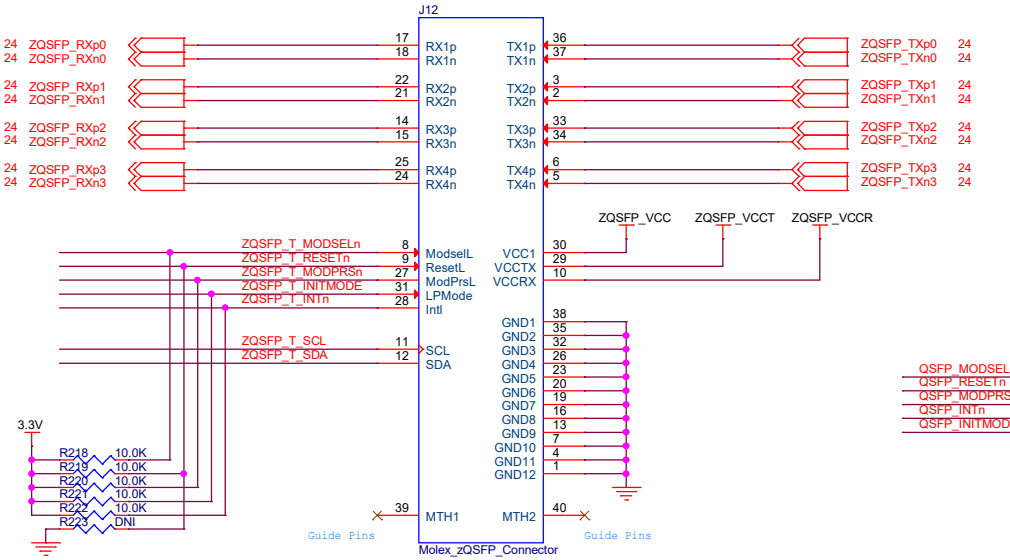
zQSFP

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

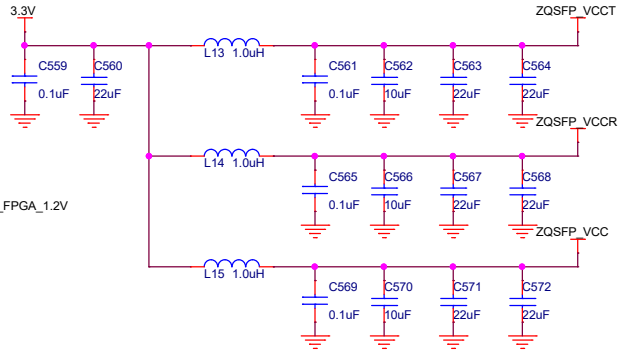
NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

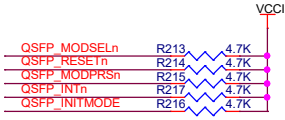
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

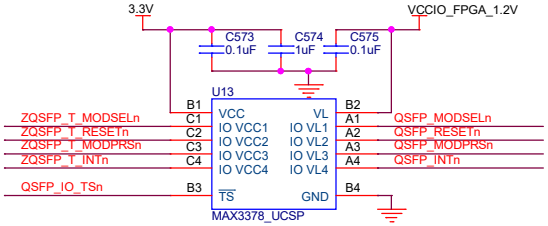


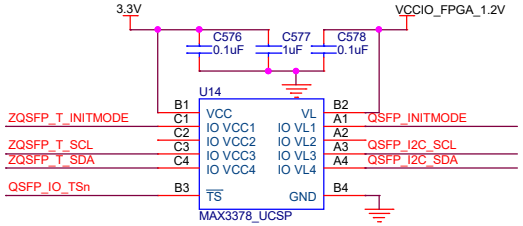
ZQSFP: Molex MPN 170432-0002

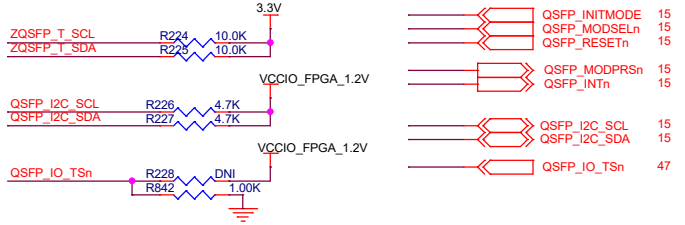


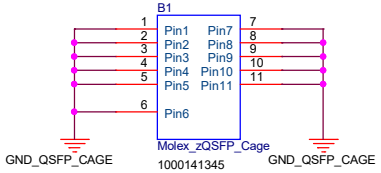
Place close to zQSFP Connector



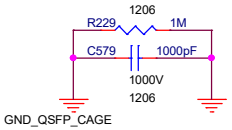








MOLEX MPN 1000141345



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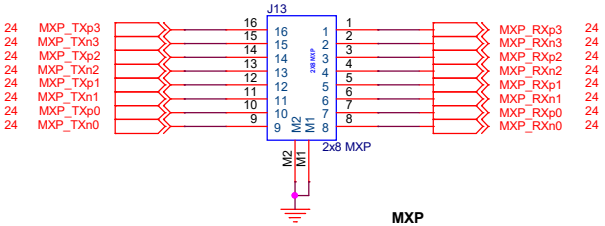
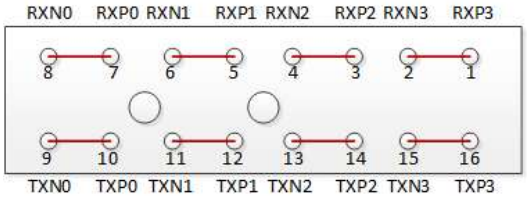
MXP / 2.4mm Connectors



MXP



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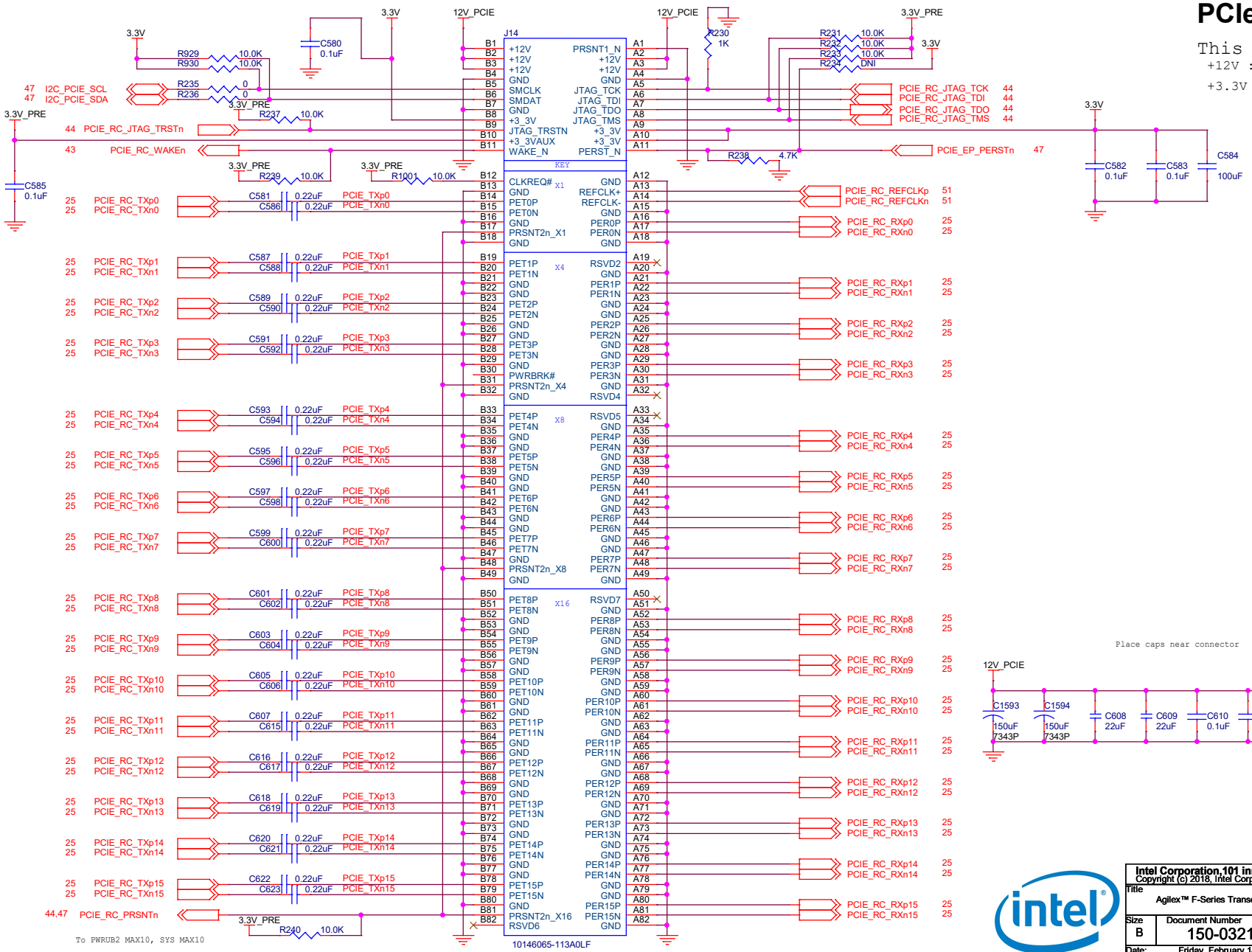
PCIe RC Connector

This is a 75W slot

+12V : 2.1A +/-8%

+3.3V : 3.0A +/-9%



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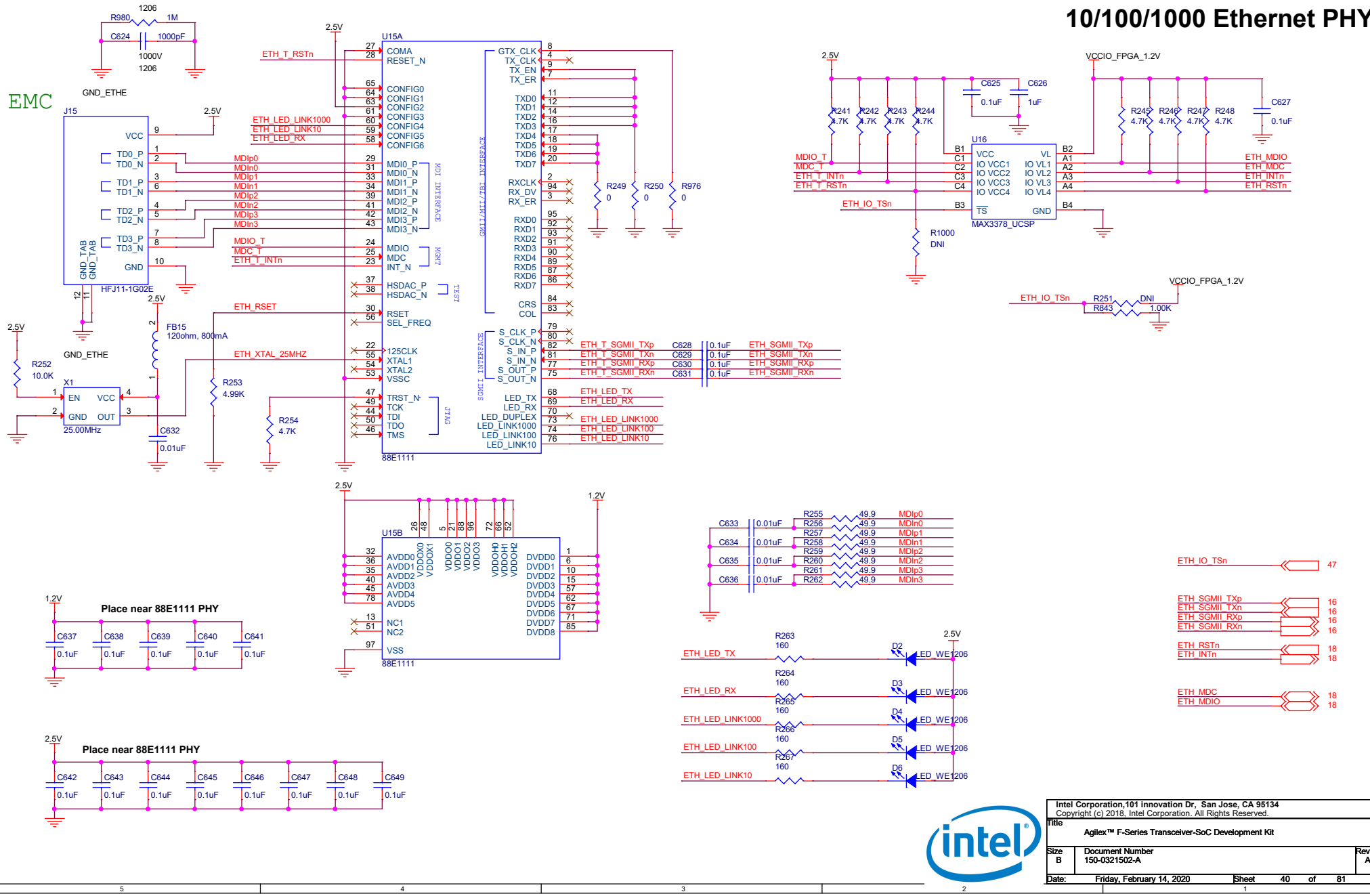
10/100/1000 Ethernet PHY



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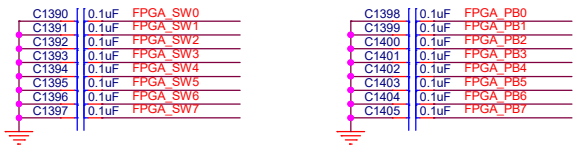
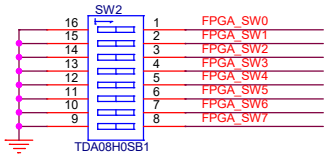
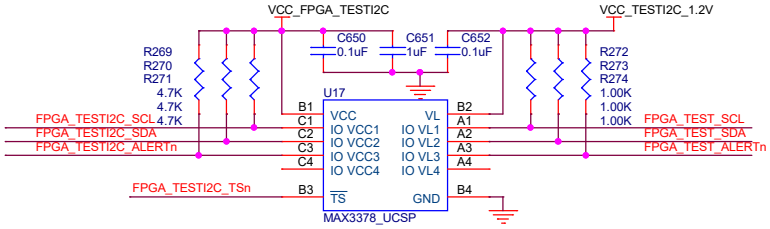
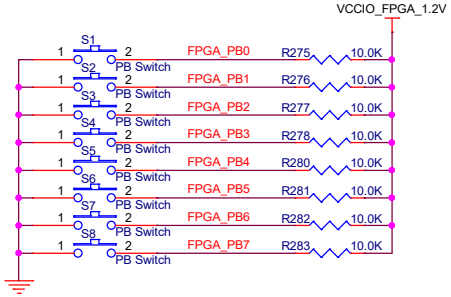
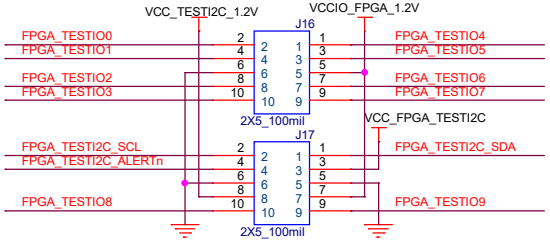
FPGA SW, PB, LED & Test IOs

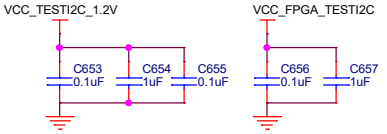


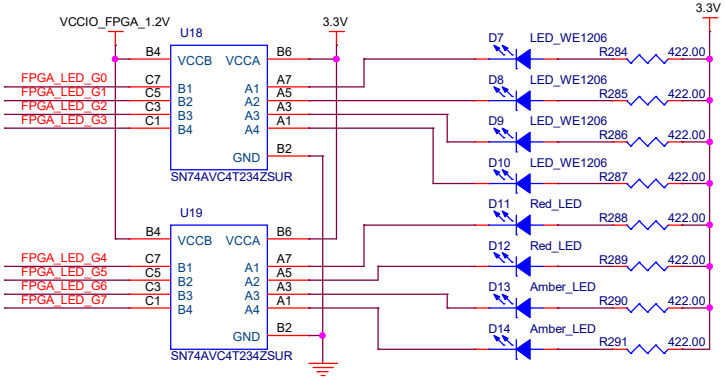


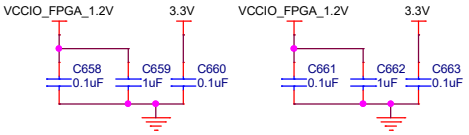


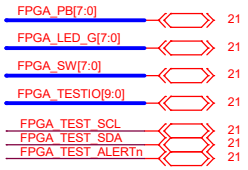












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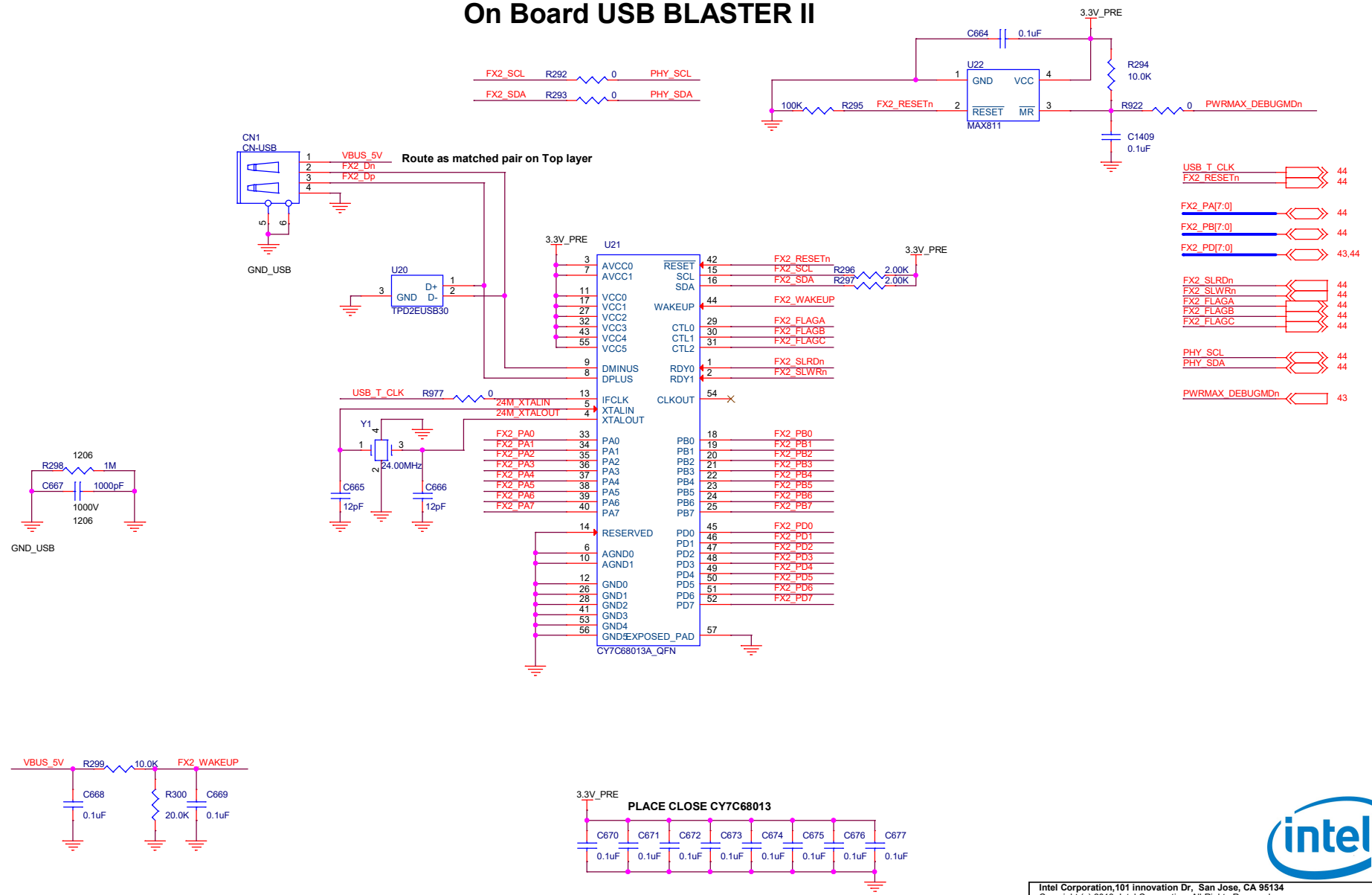
On Board USB BLASTER II



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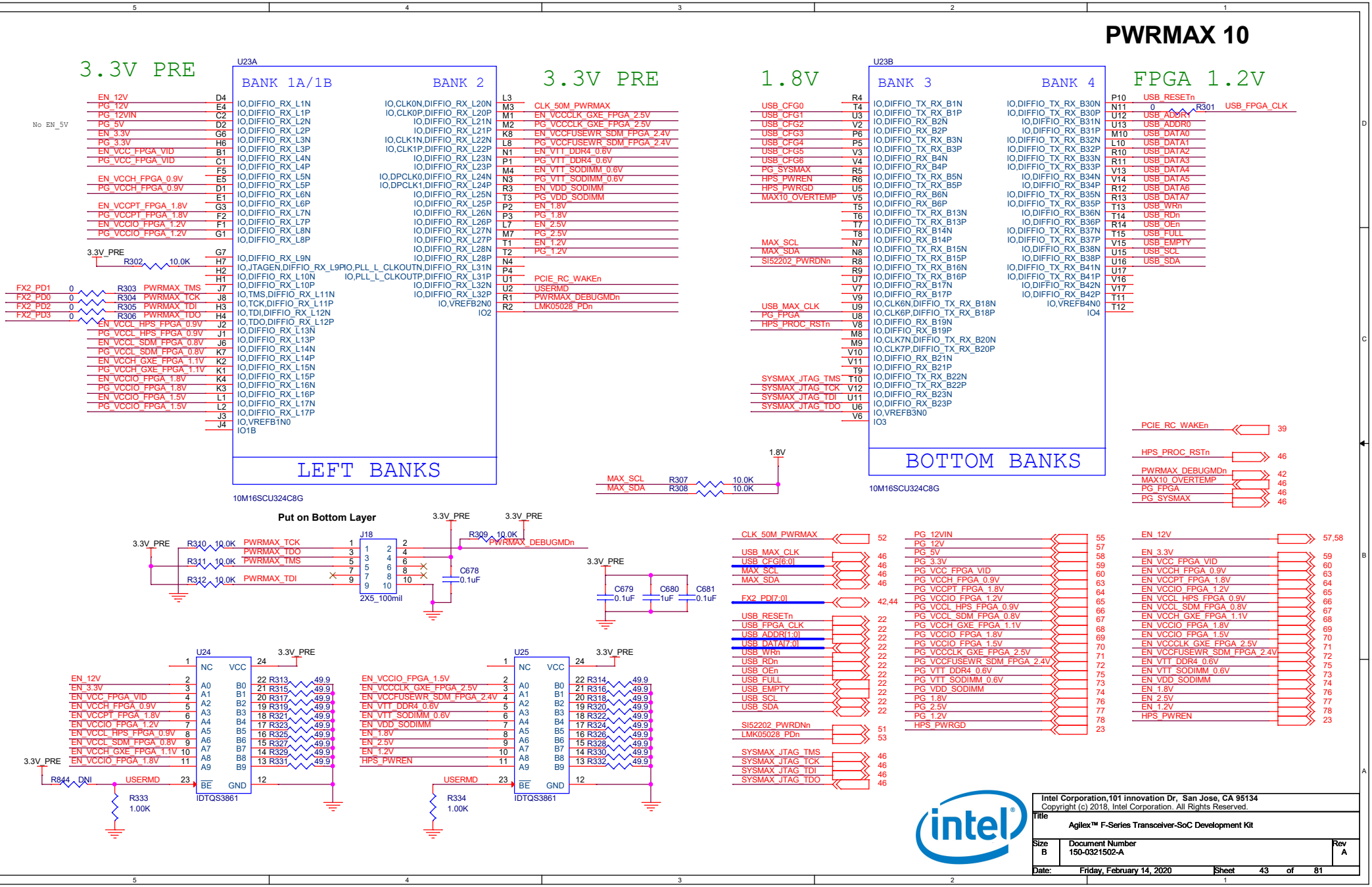
PWRMAX 10


3.3V PRE
U23A
BANK 1A/1B
BANK 2
3.3V PRE
1.8V
U23B
BANK 3
BANK 4
FPGA 1.2V
LEFT BANKS
BOTTOM BANKS
10M16SCU324C8G
10M16SCU324C8G
No EN_5V
Put on Bottom Layer
J18
2X5_100mil
C678
0.1uF
C679
0.1uF
C680
1uF
C681
0.1uF
U24
U25
IDTQS3861
IDTQS3861
R333
1.00K
R334
1.00K
R844 DNI
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PWRMAX 10

3.3V PRE

U23C

BANK 5

EXT_JTAG_TMS	P14
EXT_JTAG_TCK	N14
EXT_JTAG_TDI	R16
EXT_JTAG_TDO	T16
EXT_PROC_RSTn	M11
EXT_RESERVED	M12
EXT_RESERVED1	T18
BLASTER_DISn	U18
PCIE_RC_JTAG_TMS	M15
PCIE_RC_JTAG_TCK	N15
PCIE_RC_JTAG_TDI	M16
PCIE_RC_JTAG_TDO	N16
PCIE_RC_JTAG_TRSTn	P15
SYSMAX_JTAG_BYPASSn	R15
FPGA_JTAG_BYPASSn	L11
FMC_JTAG_BYPASSn	L12
PCIE_JTAG_BYPASSn	R17
RESERVED_JTAG_BYPASSn	T17
	K15
MSTR0	L15
MSTR1	K16
MSTR2	L16
PCIE_RC_PRSNTn	P18
FLASH_DC0_PRSNTn	R18
FLASH_DC1_PRSNTn	M18
HPS_DC_PRSNTn	N18
	P17
	P16

IO,RDN,DIFFIO_RX_R1N	K11
IO,RUP,DIFFIO_RX_R1P	K12
IO,DIFFIO_RX_R2N	L18
IO,DIFFIO_RX_R2P	M17
IO,DIFFIO_RX_R7N	K17
IO,DIFFIO_RX_R7P	L17
IO,DIFFIO_RX_R8N	J18
IO,DIFFIO_RX_R8P	K18
IO,DIFFIO_RX_R9N	G18
IO,DIFFIO_RX_R9P	H18
IO,DIFFIO_RX_R10N	G17
IO,DIFFIO_RX_R10P	H17
IO,DIFFIO_RX_R11N	J12
IO,DIFFIO_RX_R11P	J11
IO,DIFFIO_RX_R12N	H15
IO,DIFFIO_RX_R12P	J15
IO,DIFFIO_RX_R13N	H16
IO,DIFFIO_RX_R13P	J16
IO,DIFFIO_RX_R14N	H12
IO,DIFFIO_RX_R14P	H11
IO,DIFFIO_RX_R15N	G15
IO,DIFFIO_RX_R15P	F15
IO,DIFFIO_RX_R16N	F16
IO,DIFFIO_RX_R16P	G16
IO,DIFFIO_RX_R17N	D16
IO,DIFFIO_RX_R17P	E16
IO,VREFB5N0	E17
IO5	D18
	G12
	G11
	B18
	C18

BANK 6

IO,CLK2N,DIFFIO_RX_R18N	K11
IO,CLK2P,DIFFIO_RX_R18P	K12
IO,DIFFIO_RX_R19N	L18
IO,DIFFIO_RX_R19P	M17
IO,CLK3N,DIFFIO_RX_R20N	K17
IO,CLK3P,DIFFIO_RX_R20P	L17
IO,DIFFIO_RX_R21N	J18
IO,DIFFIO_RX_R21P	K18
IO,DIFFIO_RX_R22N	G18
IO,DIFFIO_RX_R22P	H18
IO,DIFFIO_RX_R23N	G17
IO,DIFFIO_RX_R23P	H17
IO,DIFFIO_RX_R24N	J12
IO,DIFFIO_RX_R24P	J11
IO,DIFFIO_RX_R26N	H15
IO,DIFFIO_RX_R26P	J15
IO,DIFFIO_RX_R27N	H16
IO,DIFFIO_RX_R27P	J16
IO,DPCLK2,DIFFIO_RX_R30N	H12
IO,DPCLK3,DIFFIO_RX_R30P	H11
IO,DIFFIO_RX_R31N	G15
IO,DIFFIO_RX_R31P	F15
IO,DIFFIO_RX_R32N	F16
IO,DIFFIO_RX_R32P	G16
IO,DIFFIO_RX_R33N	D16
IO,DIFFIO_RX_R33P	E16
IO,DIFFIO_RX_R34N	E17
IO,DIFFIO_RX_R34P	D18
IO,DIFFIO_RX_R35N	G12
IO,DIFFIO_RX_R35P	G11
IO,DIFFIO_RX_R36N	B18
IO,DIFFIO_RX_R36P	C18
IO,DIFFIO_RX_R37N	D15
IO,DIFFIO_RX_R37P	E15
IO,DIFFIO_RX_R38N	C17
IO,DIFFIO_RX_R38P	D17
IO,VREFB6N0	F18
IO6	E18

USB_T_CLK	
FX2_PA0	
FX2_PA1	
FX2_PA2	
FX2_PA3	
FX2_PA4	
FX2_PA5	
FX2_PA6	
FX2_PA7	
FX2_PB0	
FX2_PB1	
FX2_PB2	
FX2_PB3	
FX2_PB4	
FX2_PB5	
FX2_PB6	
FX2_PB7	
PWRMAX_PORSTn	
FX2_RESETn	
FX2_PD4	
FX2_PD5	
FX2_PD6	
FX2_PD7	
FX2_SLWRn	
FX2_SLRDn	
FX2_FLAGA	
FX2_FLAGB	
FX2_FLAGC	
PHY_SCL	
PHY_SDA	
REV0	
REV1	
REV2	
REV3	

RIGHT BANKS

10M16SCU324C8G

3.3V PRE FPGA 1.8V

U23D

BANK 7

FPGA_JTAG_TMS	D14
FPGA_JTAG_TCK	E14
FPGA_JTAG_TDI	B16
FPGA_JTAG_TDO	B17
	D13
HPS_DC_JTAG_TMS	D12
HPS_DC_JTAG_TCK	C15
HPS_DC_JTAG_TDI	C16
HPS_DC_JTAG_TDO	A14
HPS_DC_RESETn	A15
	C13
	C14
	B13
	B14
	F12
	F11
	B12
	C12
	B11
	C11
	A12
	A13
	A16
	A17

IO,DIFFIO_RX_T1N	D9
IO,DIFFIO_RX_T1P	D10
IO,DIFFIO_RX_T2N	A10
IO,DIFFIO_RX_T2P	A11
IO,DIFFIO_RX_T9N	G10
IO,DIFFIO_RX_T9P	F10
IO,DIFFIO_RX_T10N	A8
IO,DIFFIO_RX_T10P	A9
IO,DIFFIO_RX_T11N	B8
IO,DIFFIO_RX_T11P	B9
IO,DIFFIO_RX_T12N	C9
IO,DIFFIO_RX_T12P	C10
IO,DIFFIO_RX_T13N	D7
IO,DIFFIO_RX_T13P	D8
IO,DIFFIO_RX_T20N	A5
IO,DIFFIO_RX_T20P	A6
IO,DIFFIO_RX_T21N	B5
IO,DIFFIO_RX_T21P	C6
IO,DIFFIO_RX_T22N	C7
IO,DIFFIO_RX_T22P	C8
IO,DIFFIO_RX_T23N	C4
IO,DIFFIO_RX_T23P	C5
IO,VREFB7N0	B4
IO7	A4
	H8
	G8
	B3
	A3
	D5
	D6
	B2
	A2
	G9
	H9
	B7
	A7

BANK 8

IO,CLK4N,DIFFIO_RX_T24N	D9
IO,CLK4P,DIFFIO_RX_T24P	D10
IO,DIFFIO_RX_T25N	A10
IO,DIFFIO_RX_T25P	A11
IO,CLK5N,DIFFIO_RX_T26N	G10
IO,CLK5P,DIFFIO_RX_T26P	F10
IO,DIFFIO_RX_T27N	A8
IO,DIFFIO_RX_T27P	A9
IO,DEV_CLRN,DIFFIO_RX_T28N	B8
IO,DIFFIO_RX_T28P	B9
IO,DIFFIO_RX_T29N	C9
IO,DIFFIO_RX_T29P	C10
IO,DIFFIO_RX_T30N	D7
IO,DEV_OE,DIFFIO_RX_T30P	D8
IO,DIFFIO_RX_T31N	A5
IO,DIFFIO_RX_T31P	A6
IO,DIFFIO_RX_T32N	B5
IO,DIFFIO_RX_T32P	C6
IO,DIFFIO_RX_T33N	C7
IO,DIFFIO_RX_T33P	C8
IO,CRC_ERROR,DIFFIO_RX_T34N	C4
IO,DIFFIO_RX_T34P	C5
IO,DIFFIO_RX_T35N	B4
IO,DIFFIO_RX_T35P	A4
IO,CONF_DONE,DIFFIO_RX_T36N	H8
IO,NSTATUS,DIFFIO_RX_T36P	G8
IO,DIFFIO_RX_T37N	B3
IO,DIFFIO_RX_T37P	A3
IO,DIFFIO_RX_T38N	D5
IO,DIFFIO_RX_T38P	D6
IO,DIFFIO_RX_T39N	B2
IO,DIFFIO_RX_T39P	A2
IO,CONFIG_SEL	G9
INPUT_ONLY,NCONFIG	H9
IO,VREFB8N0	B7
IO8	A7

PWRMAX_SW0	
PWRMAX_SW1	
PWRMAX_SW2	
PWRMAX_SW3	
PWRMAX_SW4	
PWRMAX_SW5	
PWRMAX_PB0	
PWRMAX_LED_G0	
PWRMAX_LED_G1	
PWRMAX_LED_R0	
PWRMAX_LED_R1	
VCCFUSEWR_SDM_FPGA_2.4V_SET	
SODIMM_VDD_1p35V_SET	
SODIMM_VDD_1p3V_SET	
3.3V_PRE	
R335 10.0K	
R336 10.0K	
JTAG_RX	
JTAG_TX	
SC_RX	
SC_TX	
SODIMM_TYPE0	
SODIMM_TYPE1	
R337 10.0K	
R338 10.0K	

TOP BANKS

10M16SCU324C8G

3.3V_PRE

C682 0.1uF
C683 1uF
C684 0.1uF

USB_T_CLK	42
FX2_RESETn	42
FX2_PA[7:0]	42
FX2_PB[7:0]	42
FX2_PD[7:0]	42,43
FX2_SLRDn	42
FX2_SLWRn	42
FX2_FLAGA	42
FX2_FLAGB	42
FX2_FLAGC	42
PHY_SCL	42
PHY_SDA	42
PCIE_RC_JTAG_TMS	39
PCIE_RC_JTAG_TCK	39
PCIE_RC_JTAG_TDI	39
PCIE_RC_JTAG_TDO	39
PCIE_RC_JTAG_TRSTn	39
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FPGA_JTAG_TCK	14
FPGA_JTAG_TDI	14
FPGA_JTAG_TDO	14
HPS_DC_JTAG_TMS	23
HPS_DC_JTAG_TCK	23
HPS_DC_JTAG_TDI	23
HPS_DC_JTAG_TDO	23
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FLASH_DC1_PRSNTn	35,47
HPS_DC_PRSNTn	23,47
PWRMAX_SW[5:0]	45
PWRMAX_PB0	45
PWRMAX_LED_G[1:0]	45
PWRMAX_LED_R[1:0]	45

3.3V_PRE

R340 10.0K
R341 10.0K

BLASTER_DISn
EXT_PROC_RSTn
EXT_RESERVED

J19 HDR2X5

2		1	EXT_JTAG_TCK
4		3	EXT_JTAG_TDO
6		5	EXT_JTAG_TMS
8		7	EXT_RESERVED1
10		9	EXT_JTAG_TDI

Long pin and fool proof header

Logic 0 = Device JTAG Bypass
Logic 1 = Device JTAG Enable

SW3 TDA08H0SB1

16		1	FPGA_JTAG_BYPASSn
15		2	SYSMAX_JTAG_BYPASSn
14		3	FMC_JTAG_BYPASSn
13		4	RESERVED_JTAG_BYPASSn
12		5	PCIE_JTAG_BYPASSn
11		6	MSTR0
10		7	MSTR1
9		8	MSTR2

MSTR2	MSTR1	MSTR0	Mode
ON	ON	ON	BOOT
OFF	ON	ON	FMC Master
ON	OFF	ON	Reserved
OFF	OFF	ON	Reserved
ON	ON	OFF	Reserved
OFF	ON	OFF	GUI Test
ON	OFF	OFF	MAX10A Progrm Mode
OFF	OFF	OFF	ON-board UBII

3.3V_PRE

10.0K R349 EXT_JTAG_TDI
10.0K R350 EXT_JTAG_TMS
1K R353 EXT_JTAG_TCK
R356 C686 DNI

3.3V_PRE

DNI R351 PCIE_RC_PRSNTn
DNI R354 FLASH_DC0_PRSNTn
DNI R355 FLASH_DC1_PRSNTn
DNI R357 HPS_DC_PRSNTn

3.3V_PRE

MEM_CONFIG0 R870 DNI
R871 DNI

R991 10.0K
R990 10.0K
R987 10.0K
R992 10.0K
R993 10.0K
R994 10.0K
R995 10.0K

12V_IN

SODIMM_TYPE0
SODIMM_TYPE1

U82 LM339PW

	1OUT	OUT3	14
	2OUT	OUT4	13
3	VCC	GND	12
4	2IN-	4IN+	11
5	2IN+	4IN-	10
6	1IN-	3IN+	9
7	1IN+	3IN-	8

MEM_CONFIG0
R988 10.0K
R989 10.0K

12V_IN

C1596 10uF 1206 25V
C1597 0.1uF

3.3V_PRE

C685 0.1uF

U28 MAX811

1	GND	VCC	4
2	RESET	MR	3

100K R358 PWRMAX_PORSTn

VCCFUSEWR_SDM_FPGA_2.4V_SET 72
SODIMM_VDD_1p35V_SET 74
SODIMM_VDD_1p3V_SET 74
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REV[3:0] 45

3.3V_PRE

JTAG_RX D15 R344 422.00 LED_WE1206
JTAG_TX D16 R347 422.00 LED_WE1206
SC_RX D17 R348 422.00 LED_WE1206
SC_TX D18 R352 422.00 LED_WE1206

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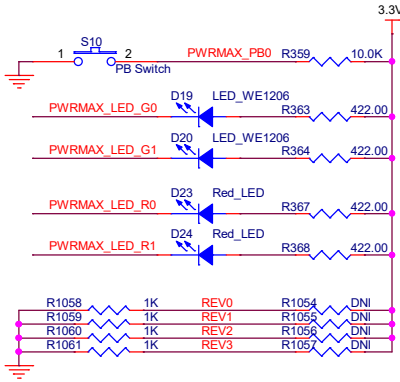
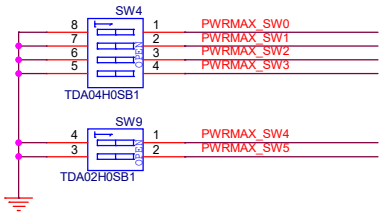
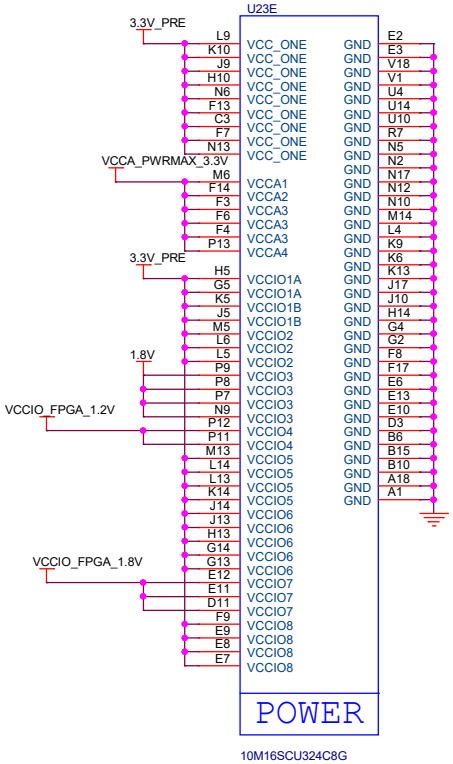
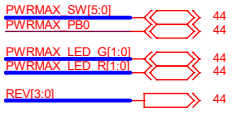
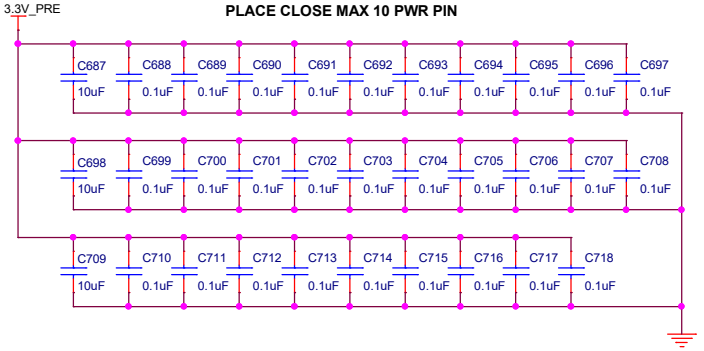
PWRMAX 10

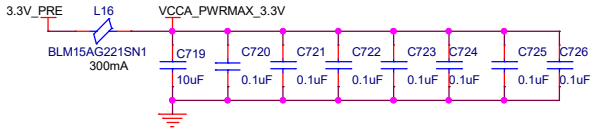


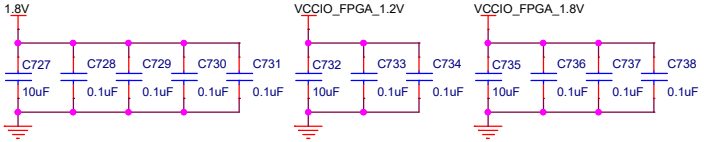












Pin	Function
SW0	Reserved
SW1	VCCFUSEWR_SDM_FPGA_2.4V_SETn
SW2	VCCL_HPS_FPGA_0.9V_BYPASS_MODEn
SW3	LMK05028_PDn
SW4	Reserved
SW5	Reserved

Pin	Function
G0	PG_FPGA
G1	PG_SYSMAX
R0	PWR_ERR
R1	Over Voltage/Current
PB0	FPGA Power Cycle

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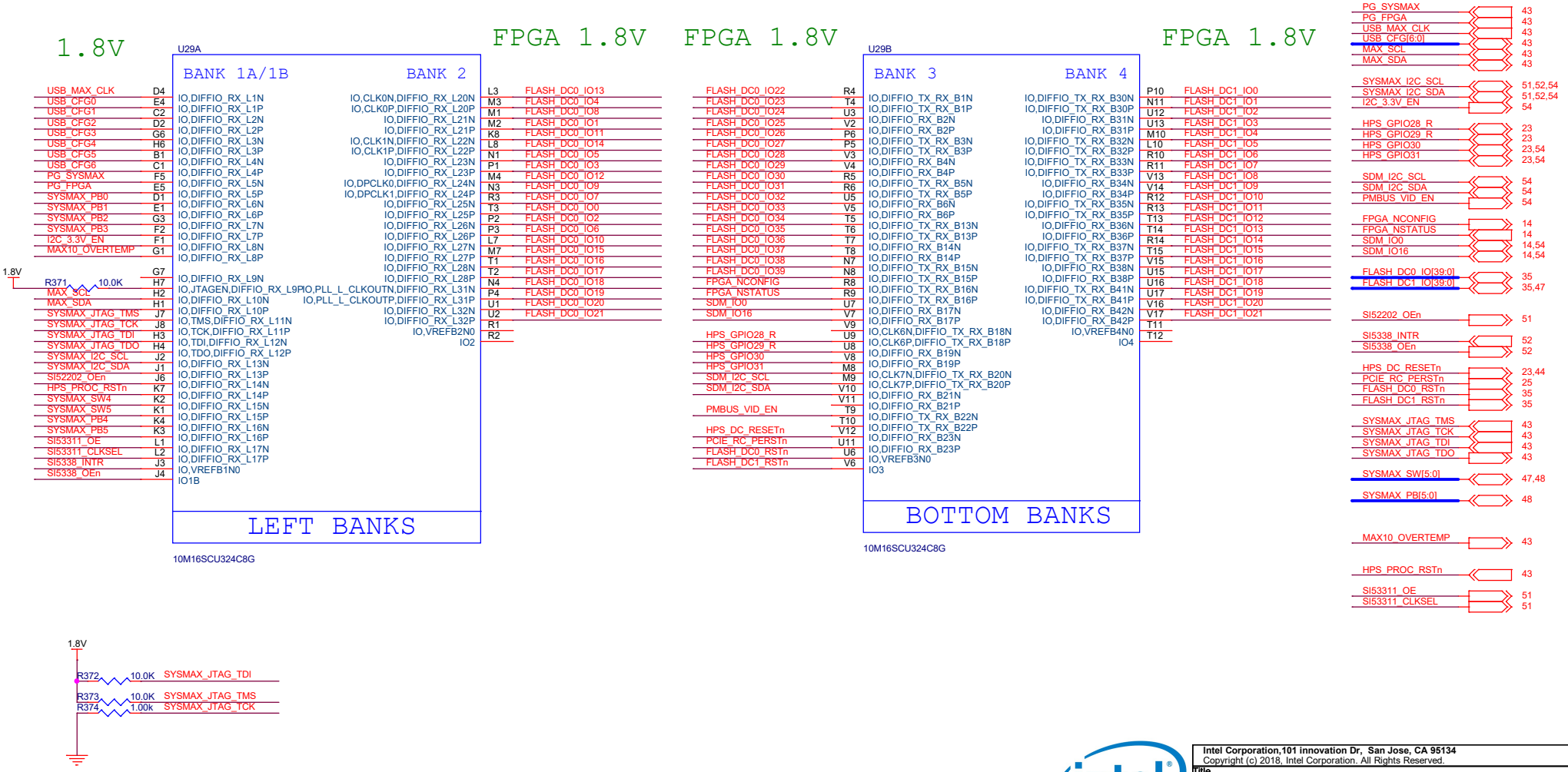
SYSMAX 10



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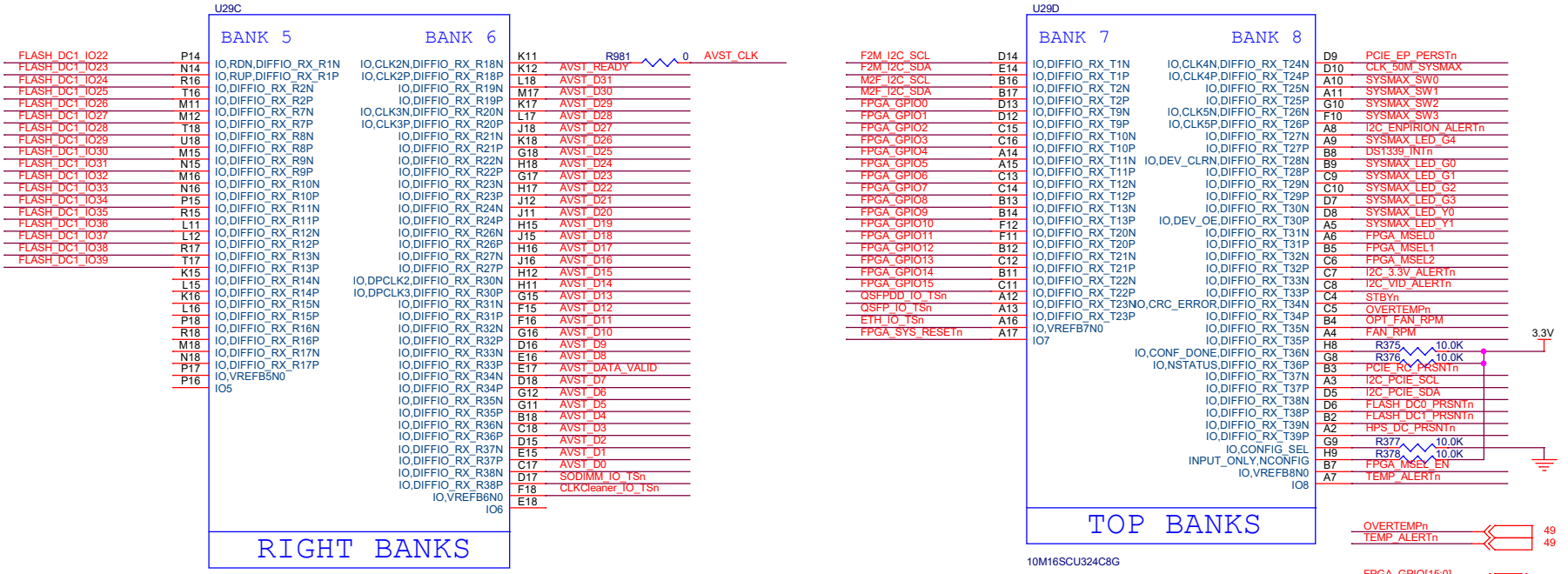
SYSMAX 10

FPGA 1.8V

FPGA 1.2V

FPGA 1.2V

3.3V



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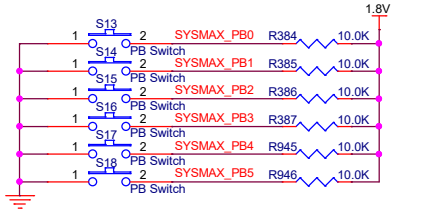
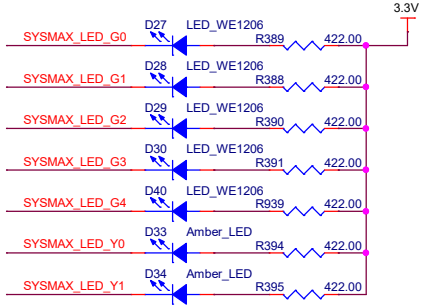
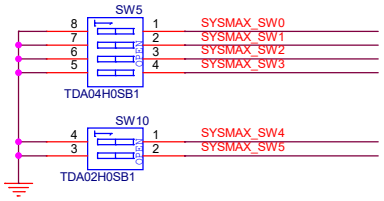
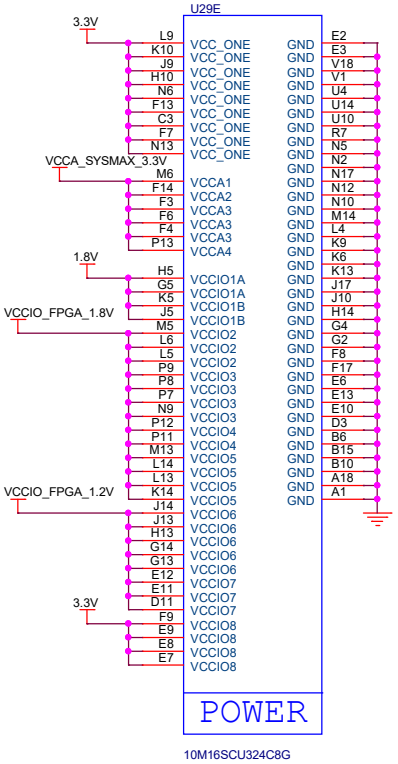
SYSMAX 10









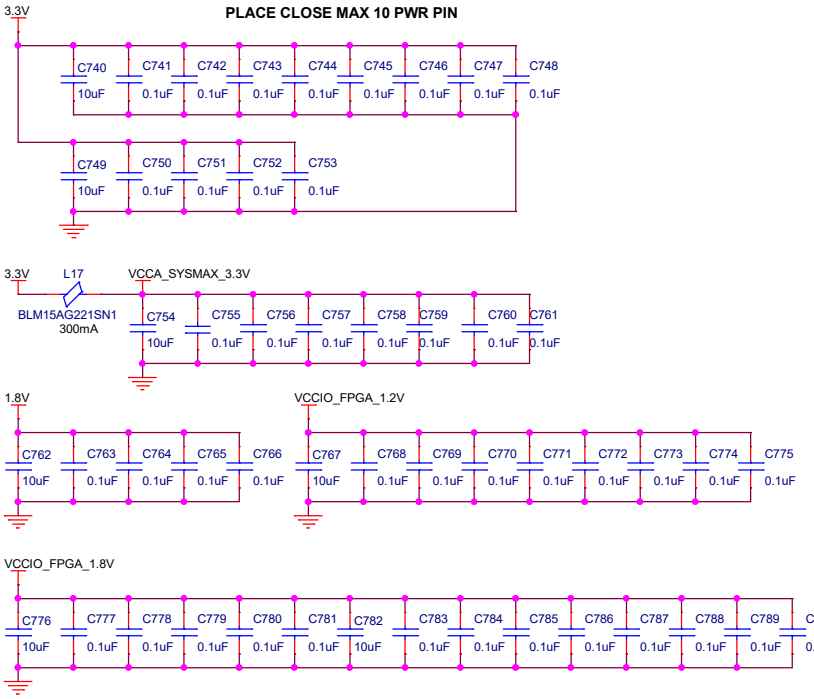
Pin	Function
SW0	FACTORY_LOADn
SW1	CLKSEL_156M
SW2	Reserved
SW3	Reserved
SW4	I2C_3.3V_BUS_DEBUG_MODEn
SW5	CLKCleaner_IO_DEBUG_MODEn

Pin	Function
G0	PGM_LED0
G1	PGM_LED1
G2	PGM_LED2
G3	MAX_LOAD
G4	MAX_CONF_DONE
Y0	MAX_ERROR
Y1	OVERTEMP

Pin	Function
PB0	MAX_RESETn
PB1	CPU_RESETn
PB2	HPS_COLD_RESETn
PB3	Reserved
PB4	PGM_SEL
PB5	PGM_CFG

SYSMAX_SW[5:0] 46,47
SYSMAX_PB[5:0] 46

SYSMAX_LED_G[4:0] 47
SYSMAX_LED_Y[1:0] 47



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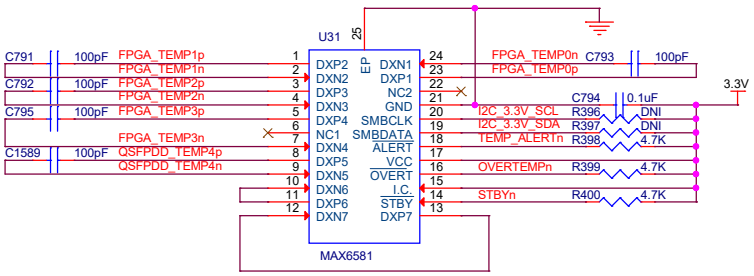
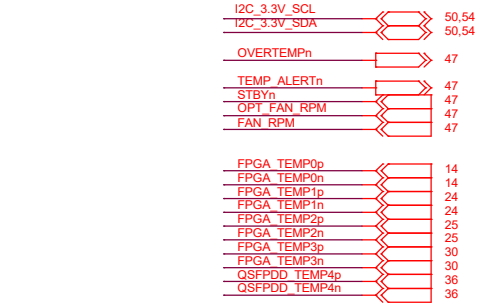
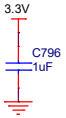
Temperature Sense/FAN

Note: TEMPDIODE instructions
- route as diff pair and less vias
- use GND guard traces
- trace width = 10mils
- trace gap = as minimum as possible
- trace length < 8inches

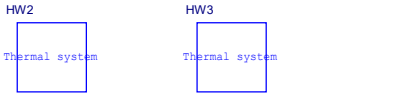
SLAVE ADDR = 1001 101



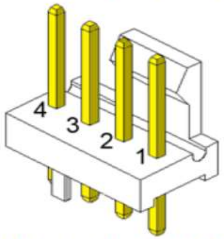




0: SDM
1: E-tile
2: P-tile
3: Core
4: QSFPDD1x1

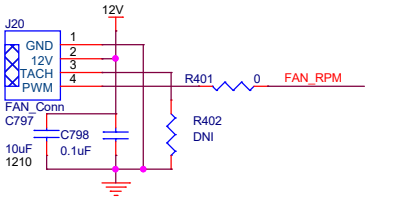


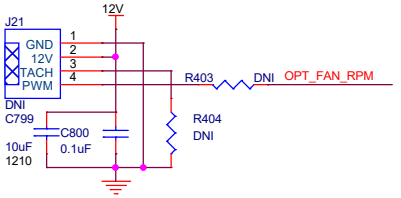
4-Wire Pulse Width Modulation (PWM) Controlled Fans



Motherboard CPU Fan 4 Pin header Connector.

Pin	Name	Color
1	GND	black
2	+12VDC	yellow
3	Sense	green
4	Control	blue





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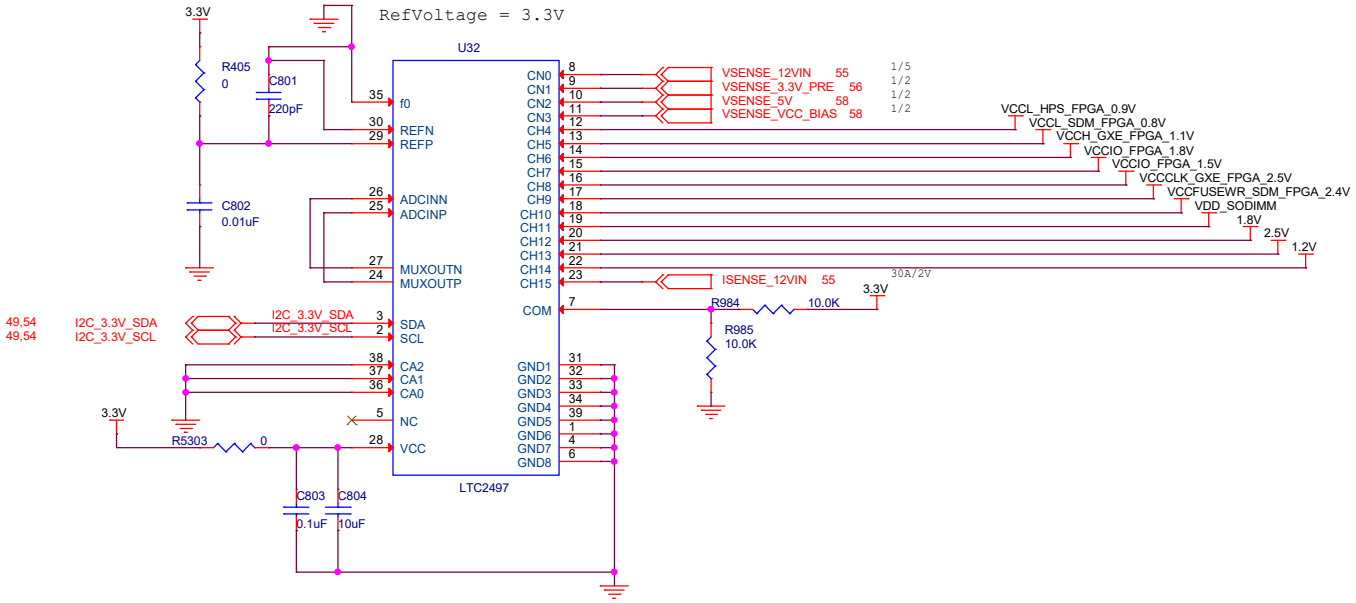
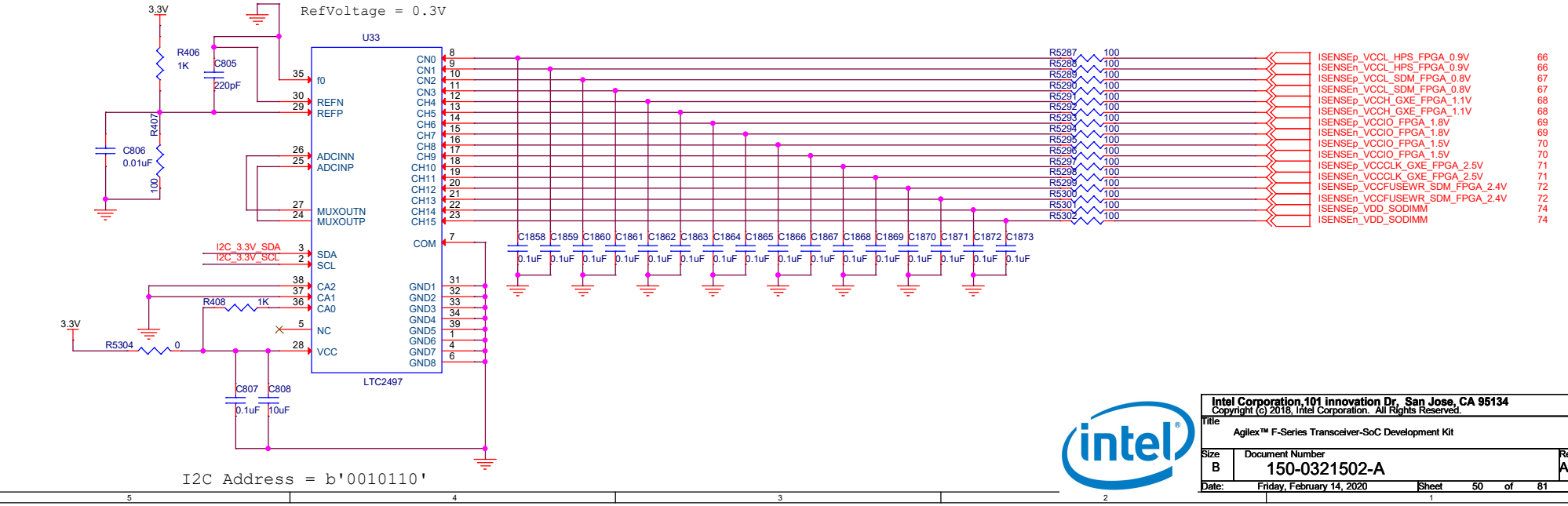
Power Monitors





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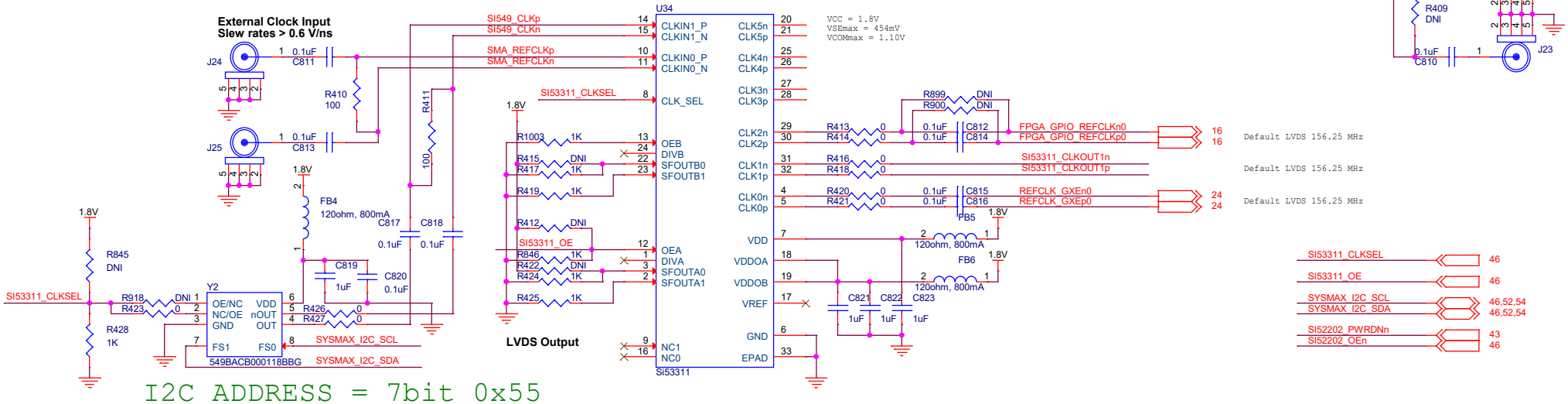
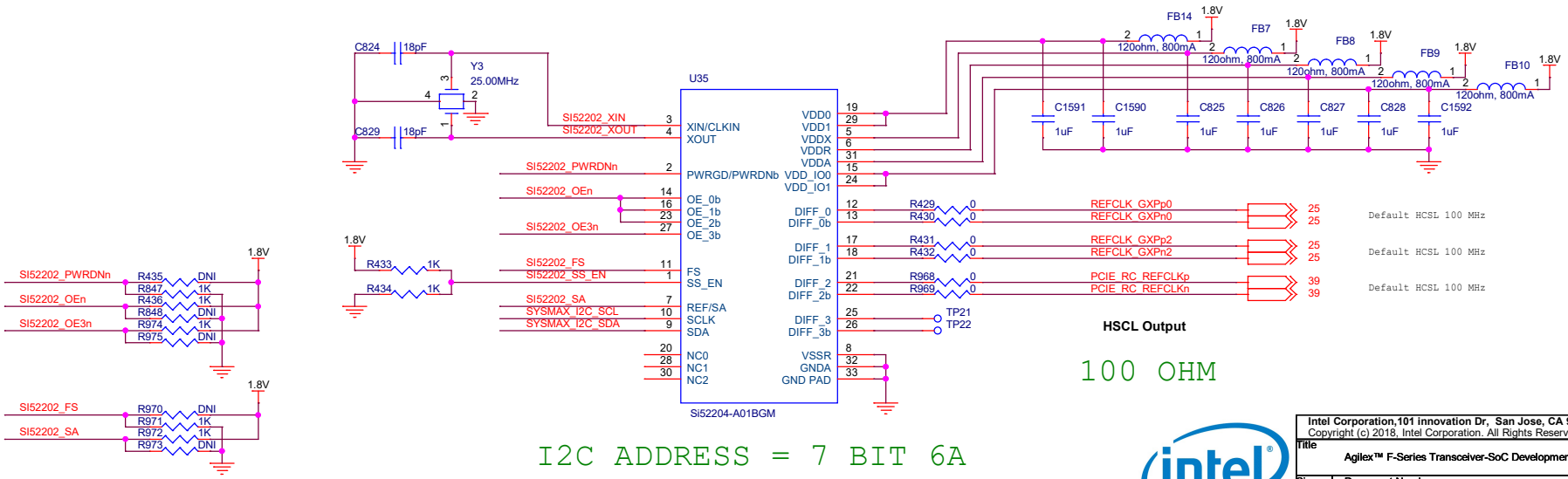
Clock 1



I2C ADDRESS = 7bit 0x55

Clock freq range 0.2M-800M
Default 156.25MHz
LVDS



100 OHM

I2C ADDRESS = 7 BIT 6A

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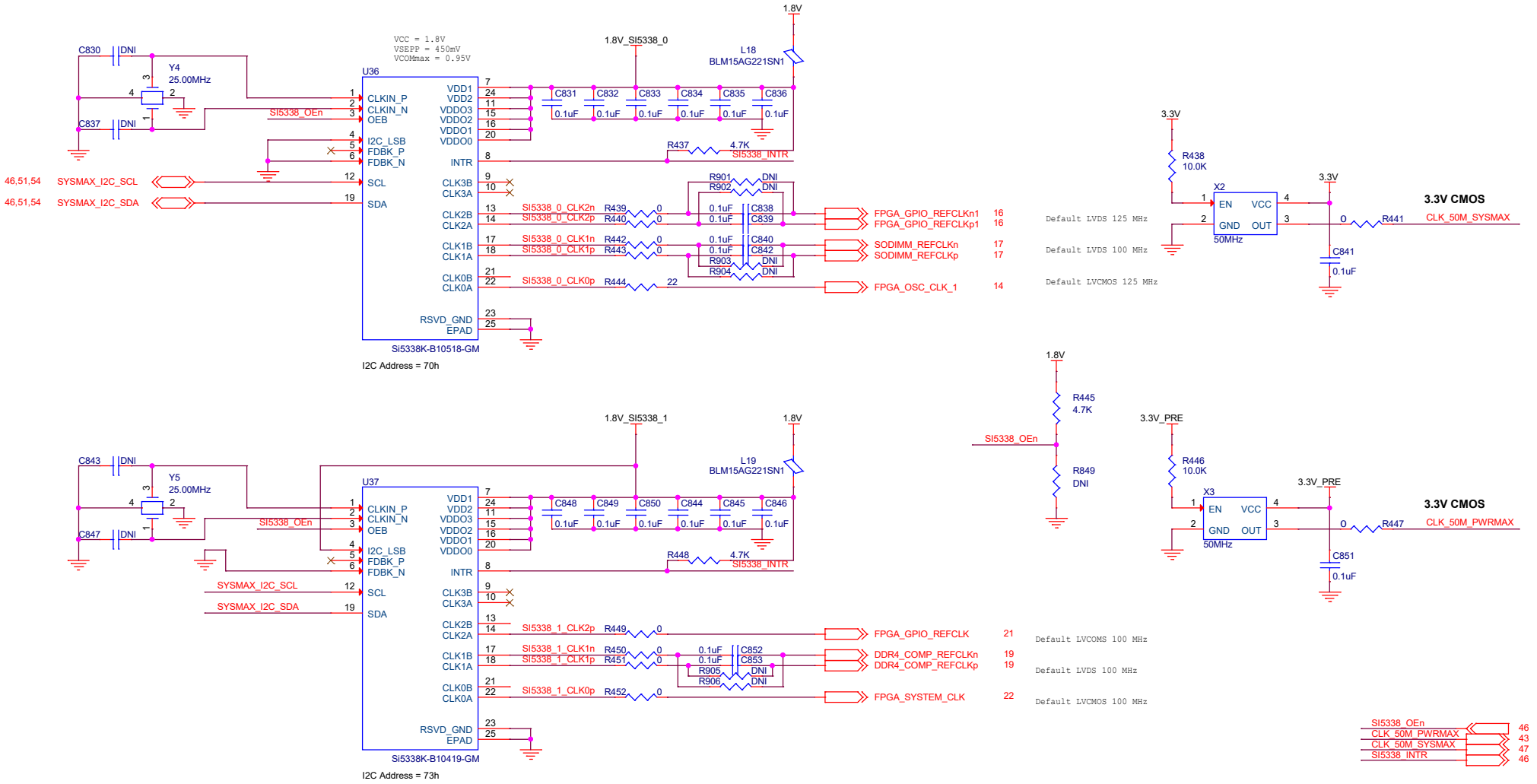
Clock 2



LVCMOS18
VOHmin = 1.50V * 2/3 = 1.00V
VOLmax = 0.30V * 2/3 = 0.20V

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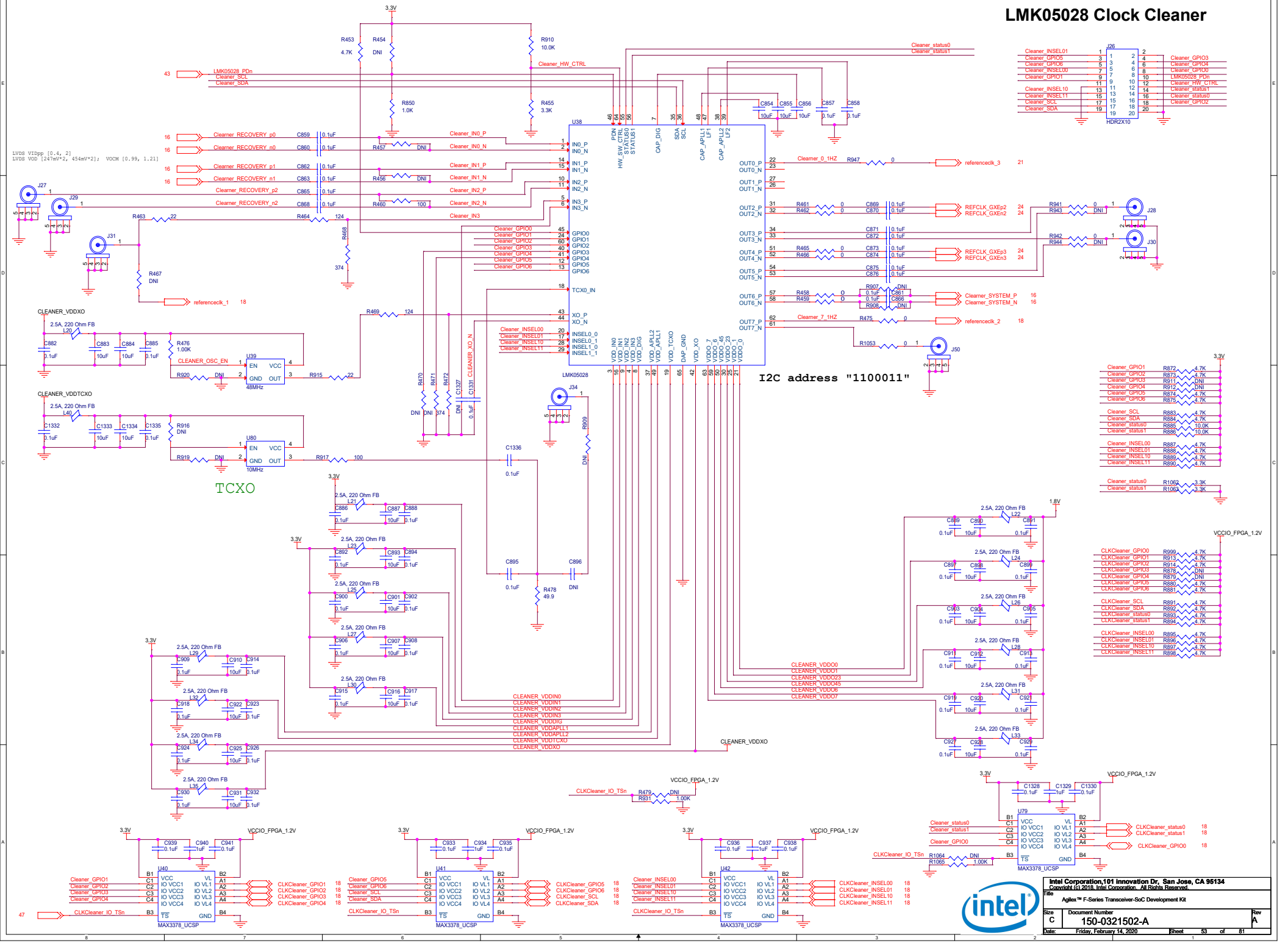
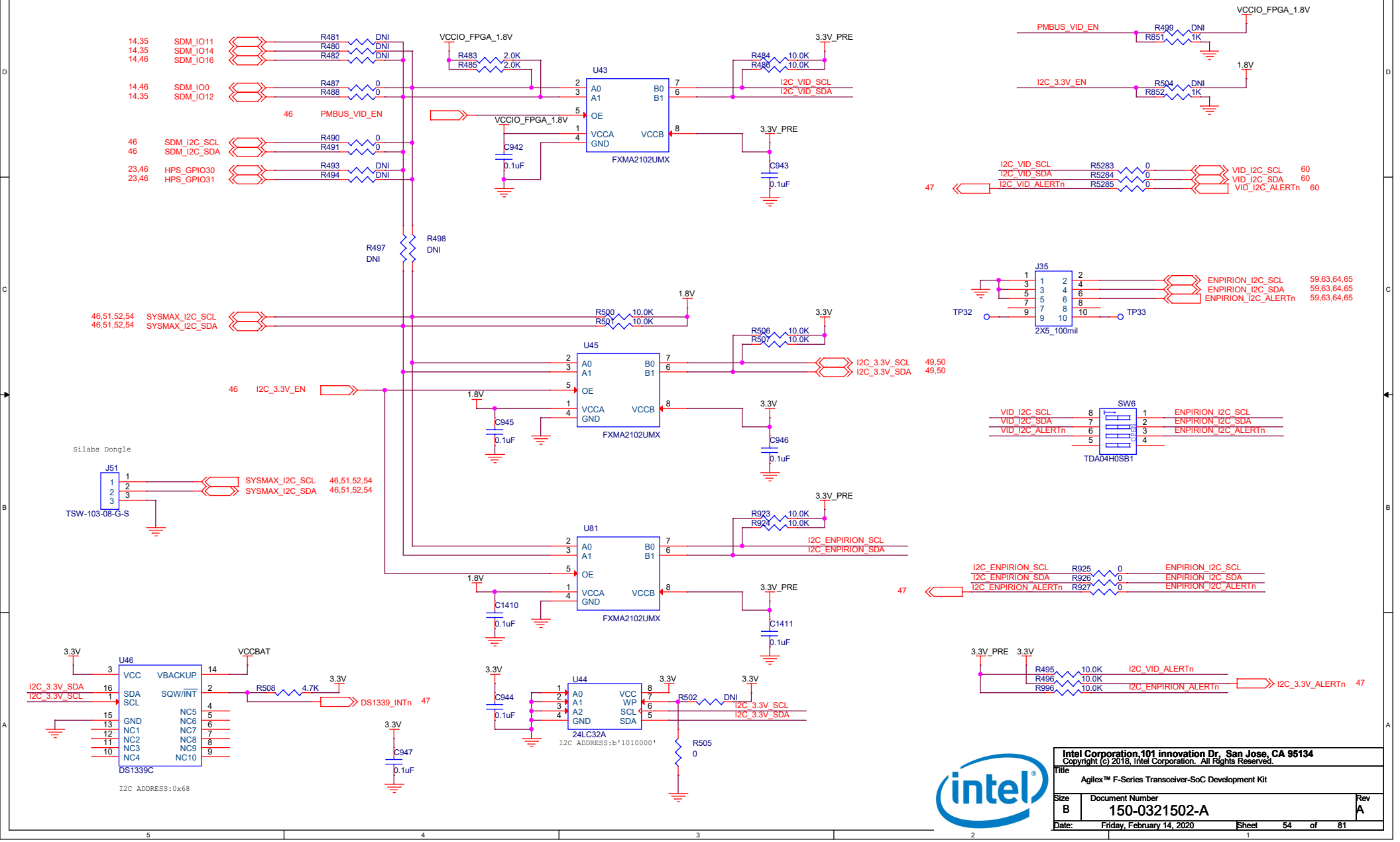
LMK05028 Clock Cleaner



I2C And PMBUS



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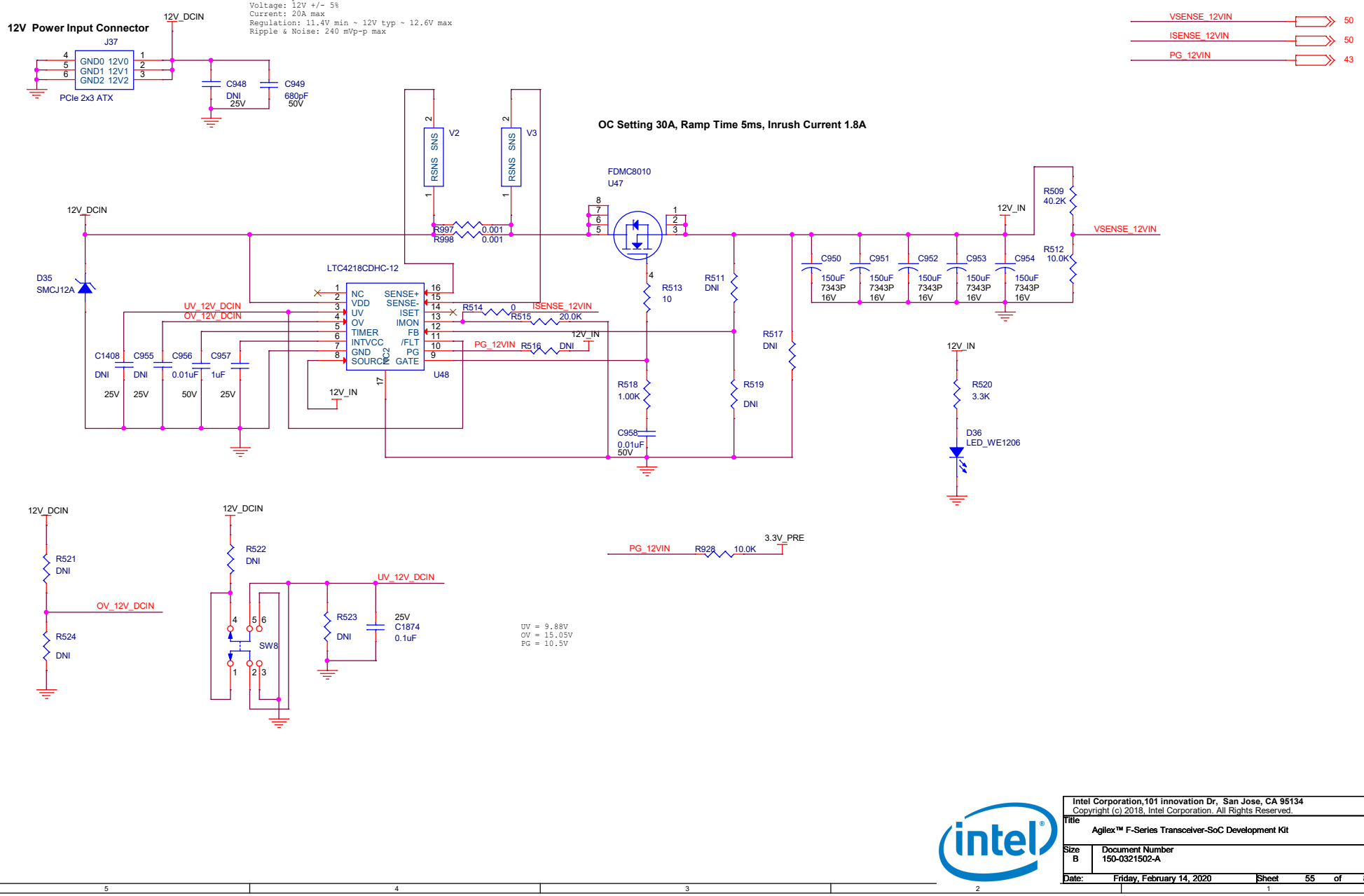
PWR - POWER INPUT



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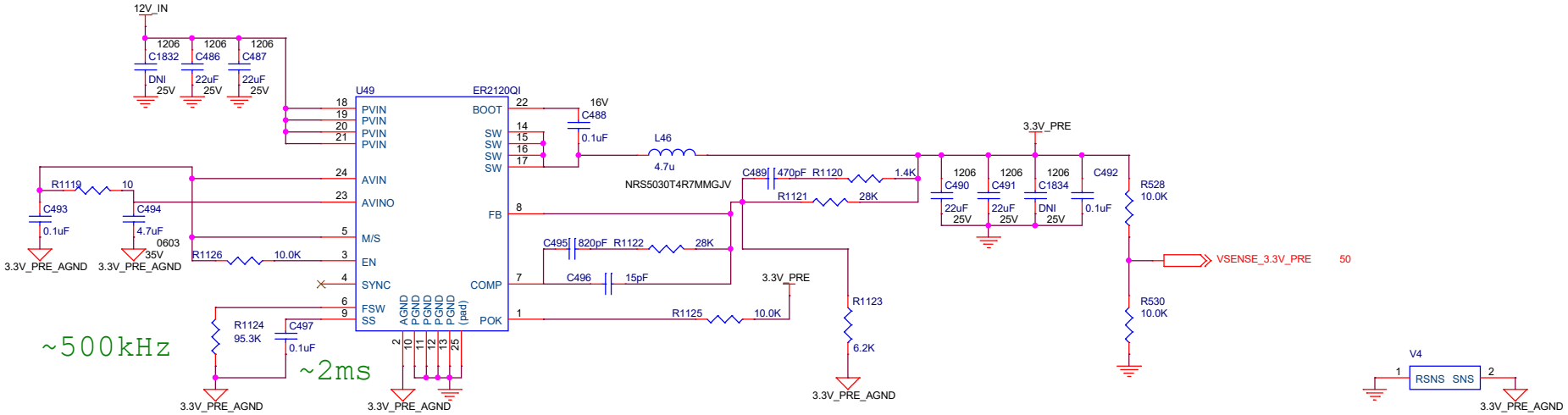
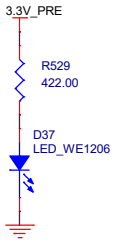
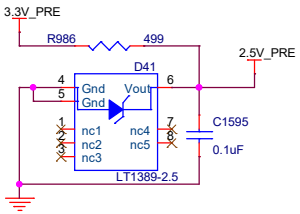
PWR - 3.3V_PRE



GND of input/output filter and PGND shall be connected to GND layer directly, while all signal GND and AGND shall be connected together and then go to a single via away from the PGND area





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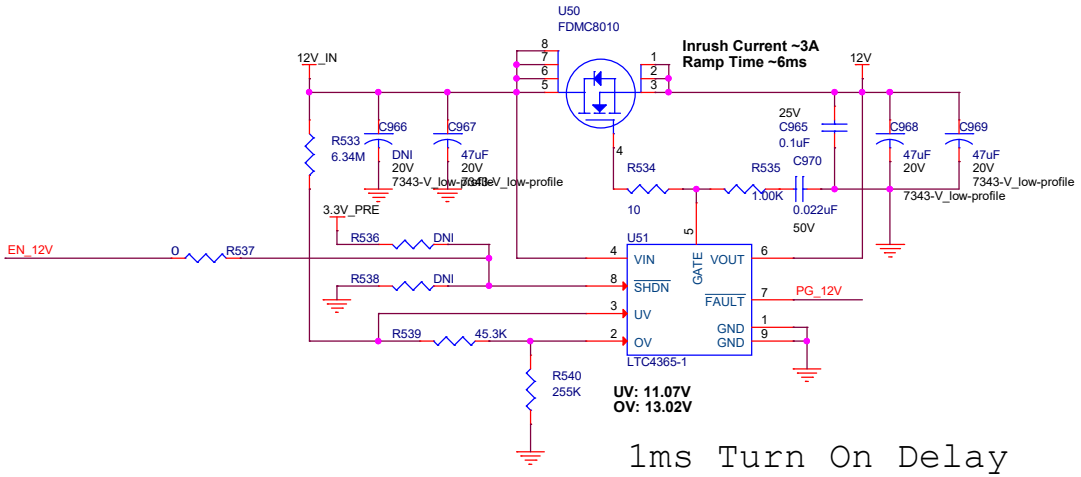
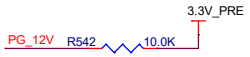
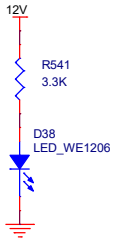
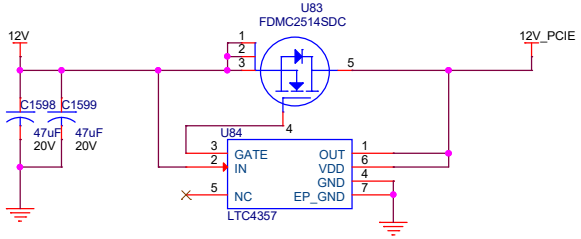
PWR - 12V



1ms Turn On Delay







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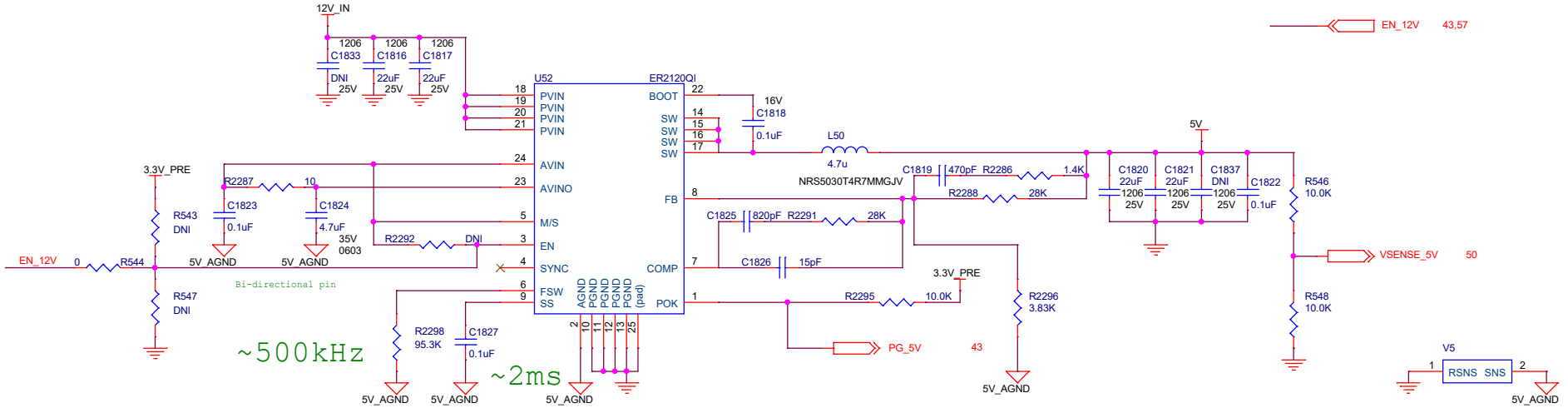
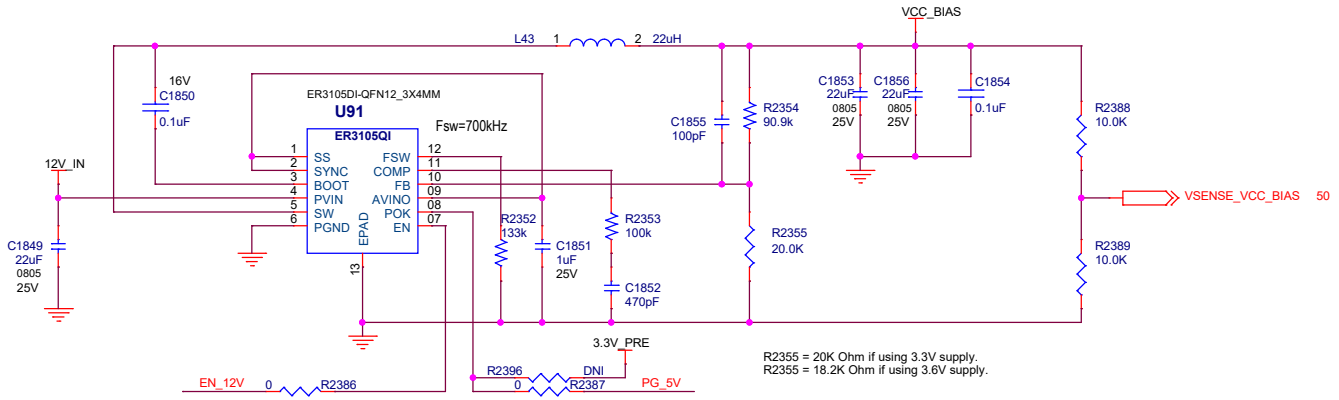
PWR - ENPIRION BIAS



GND of input/output filter and PGND shall be connected to GND layer directly, while all signal GND and AGND shall be connected together and then go to a single via away from the PGND area



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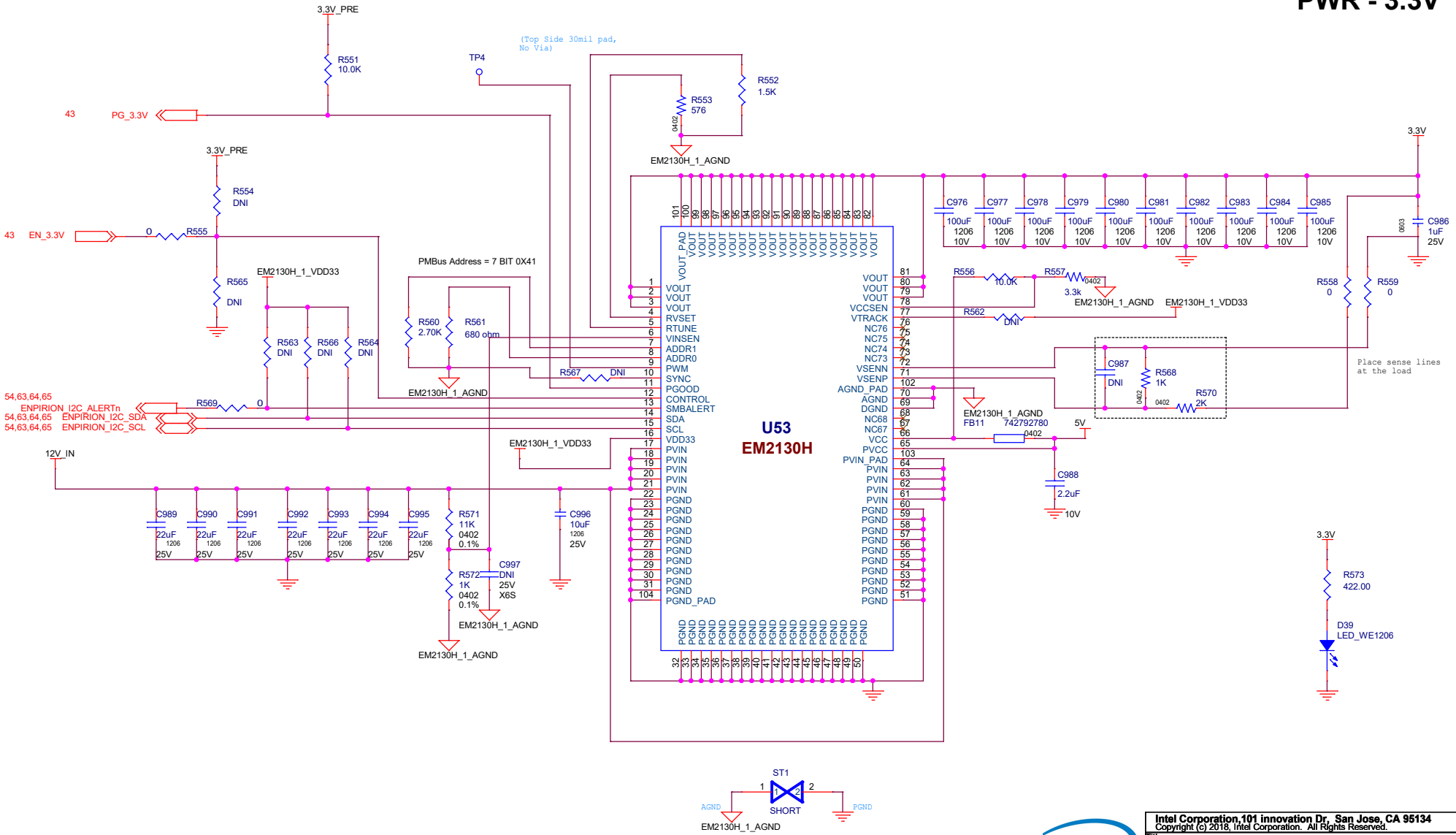
PWR - 3.3V



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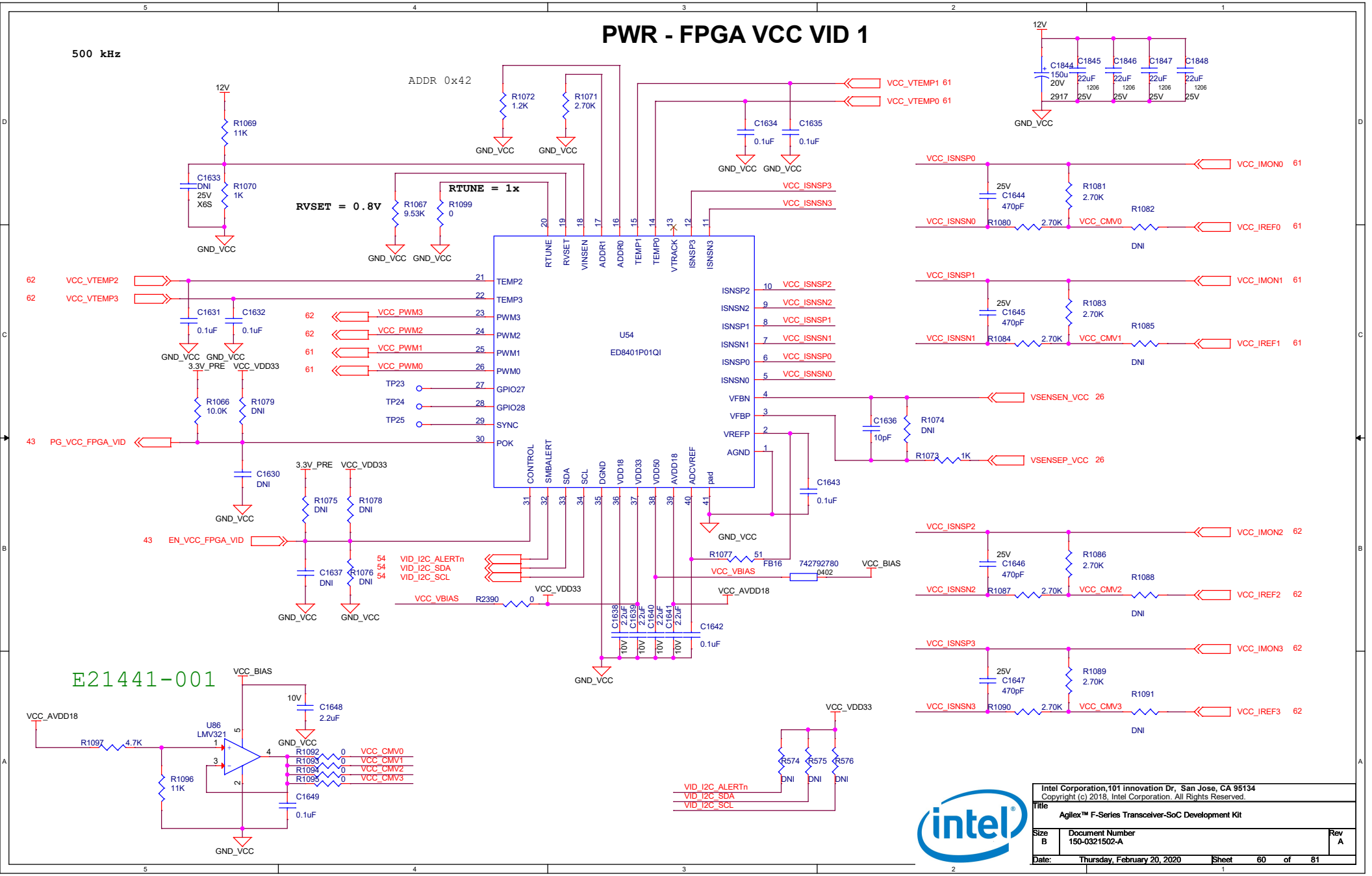
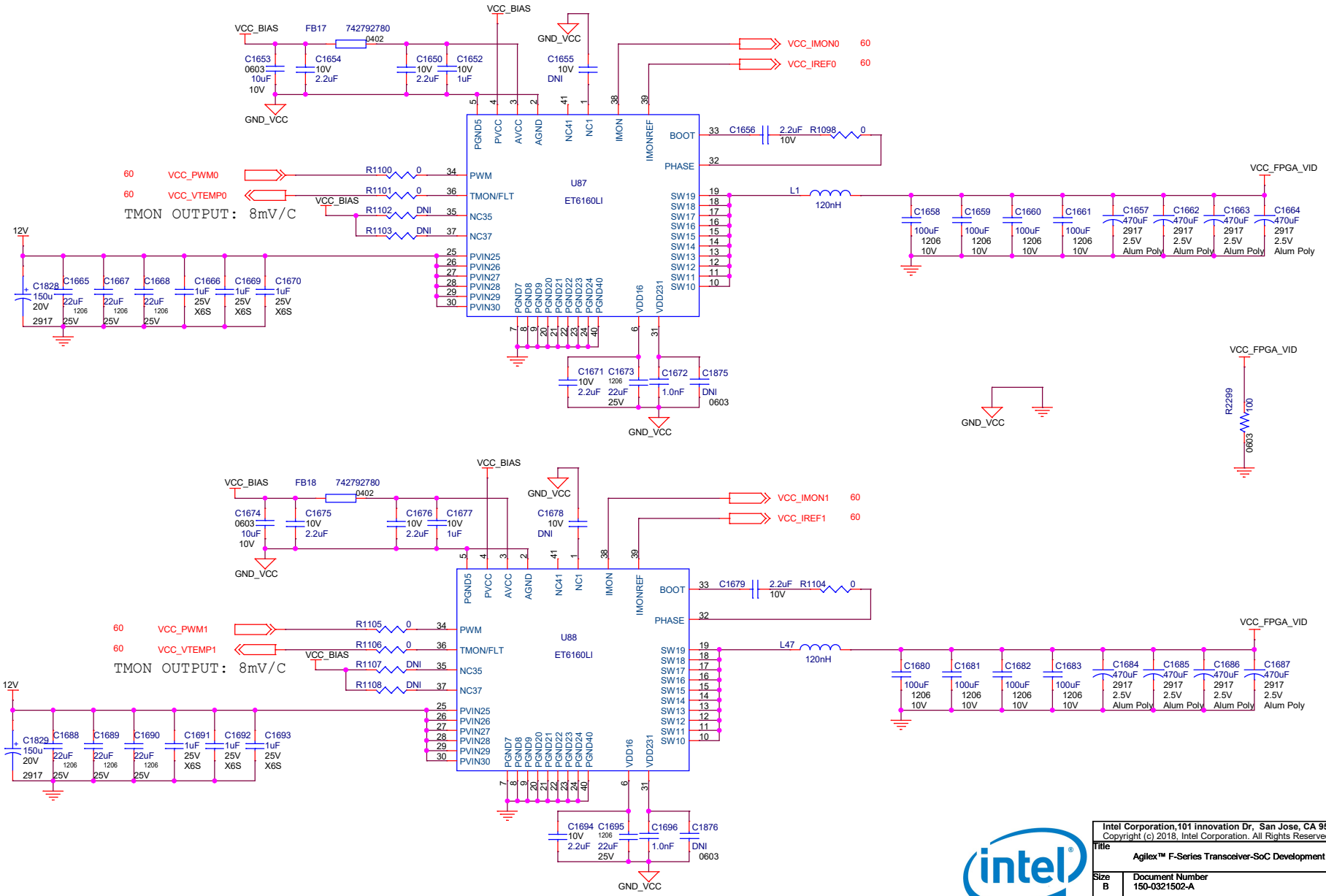
PWR - FPGA VCC VID 1

500 kHz



PWR - FPGA VCC VID 2



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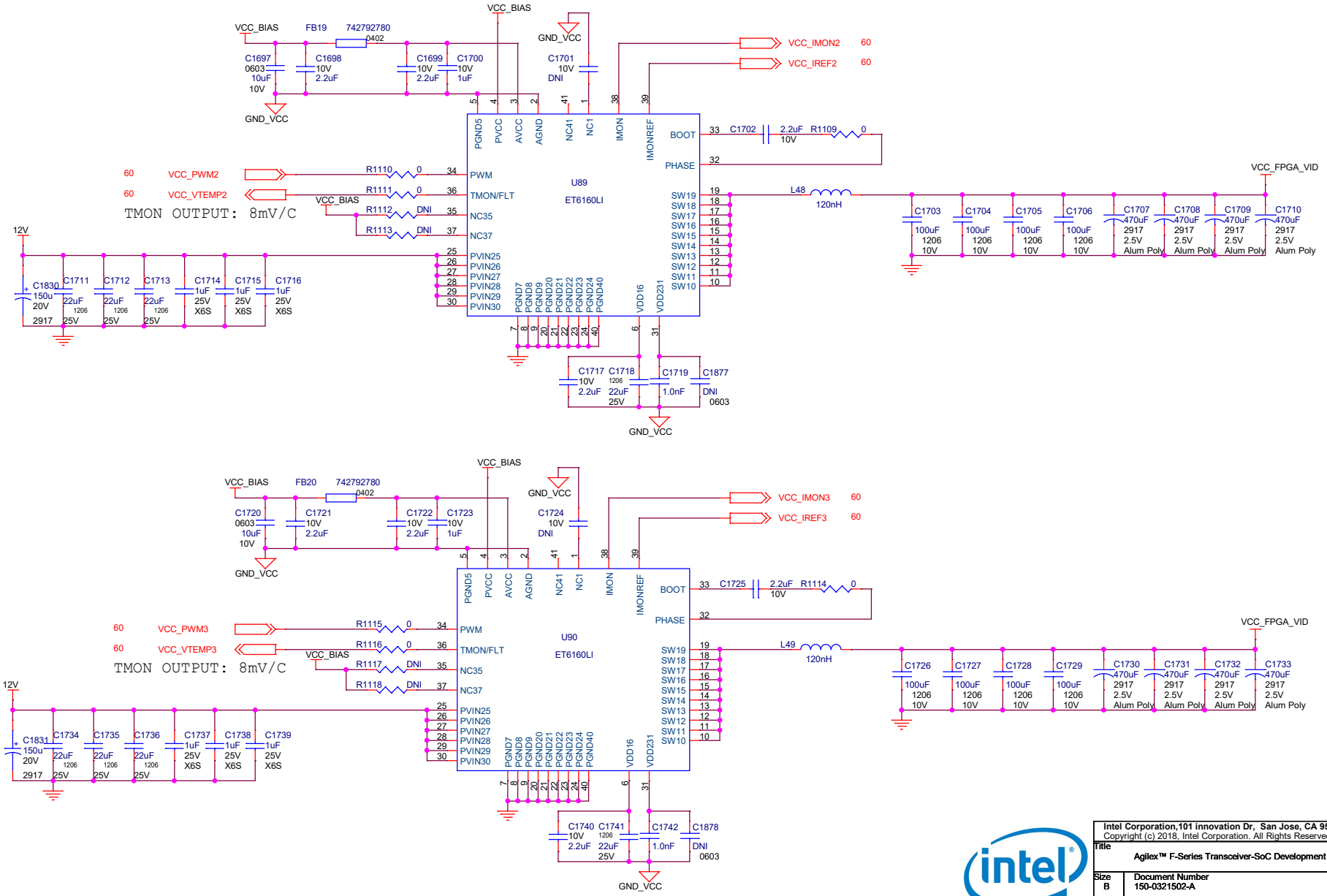
PWR - FPGA VCC VID 3



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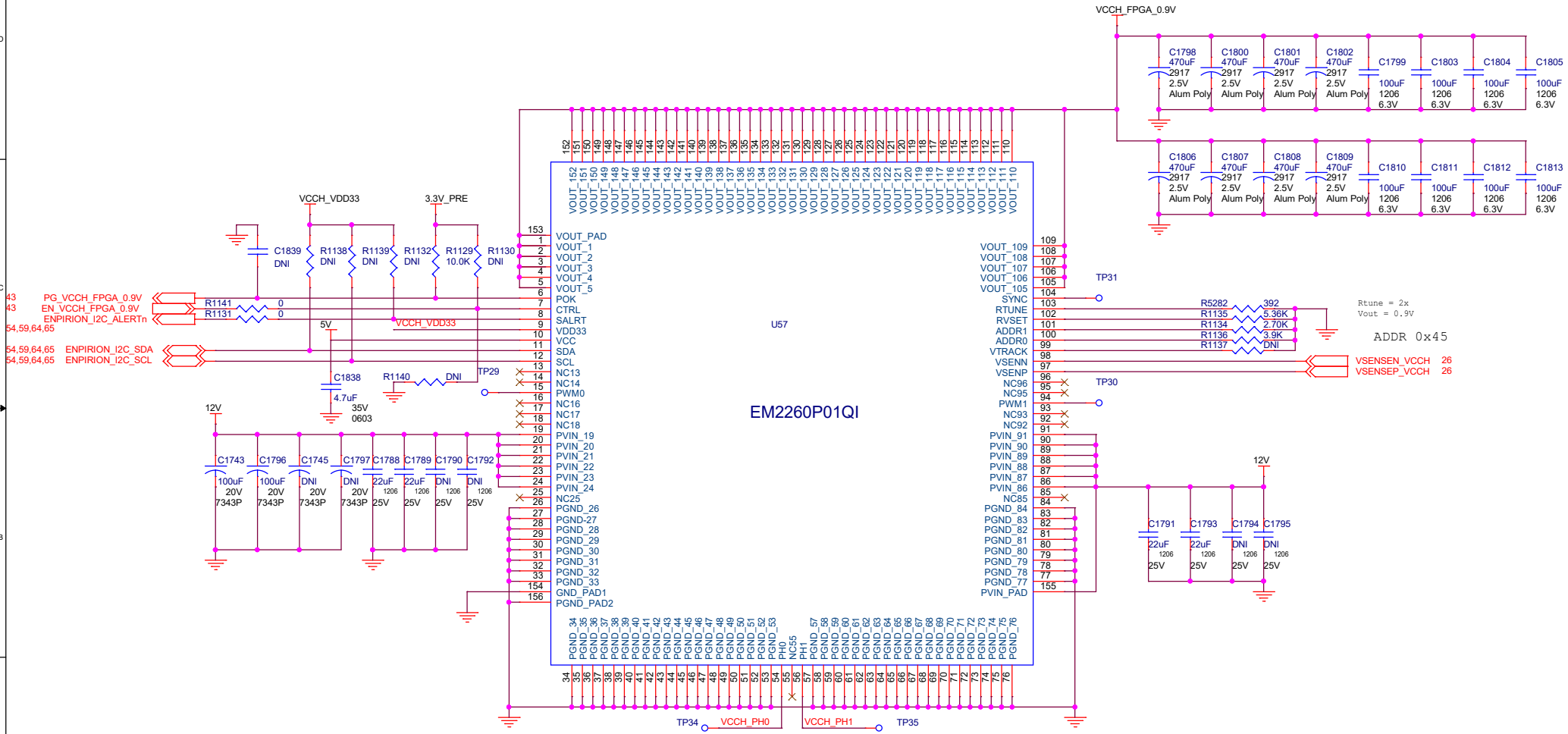
PWR - FPGA VCCH 0.9V



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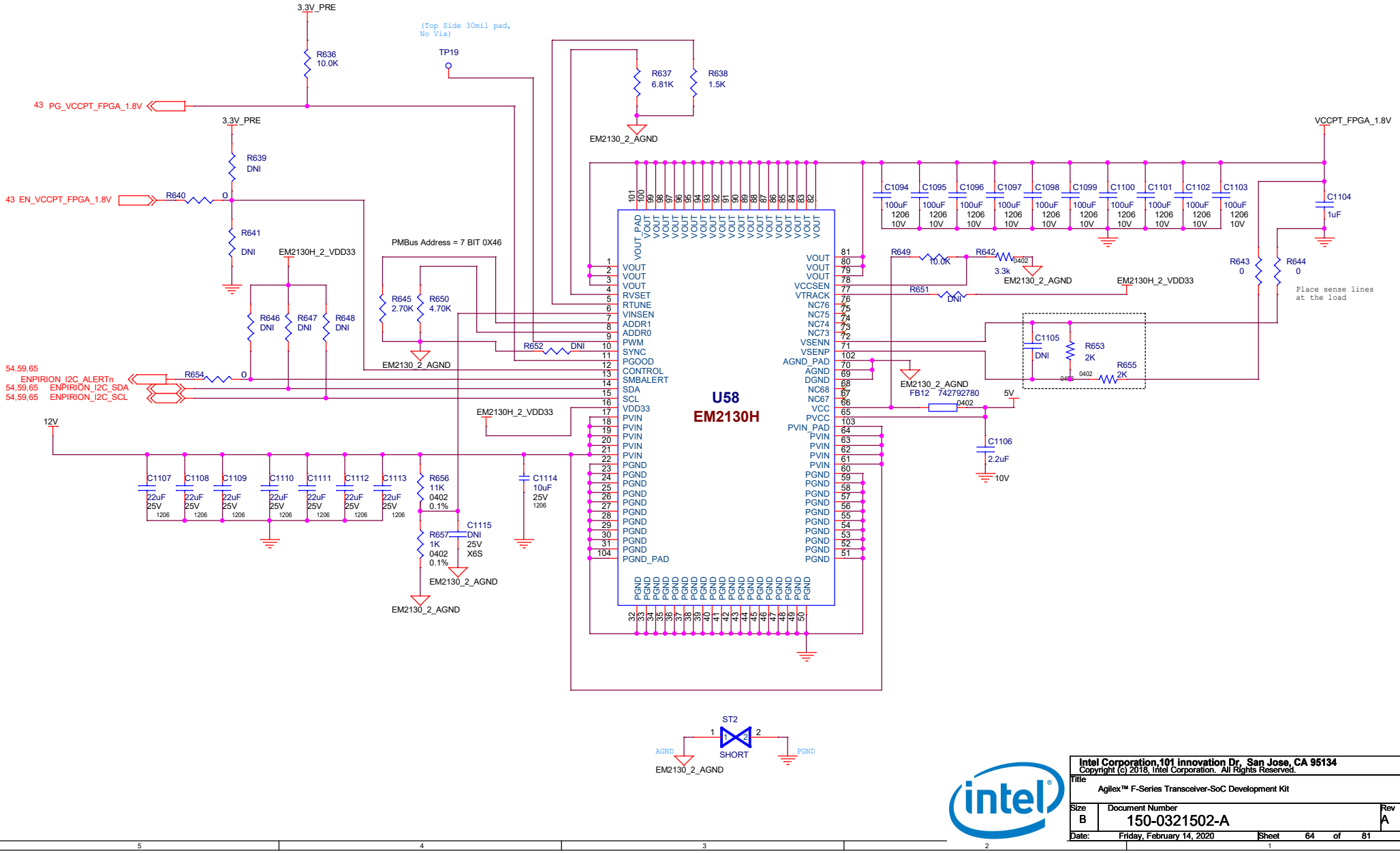
PWR - FPGA VCCPT 1.8V



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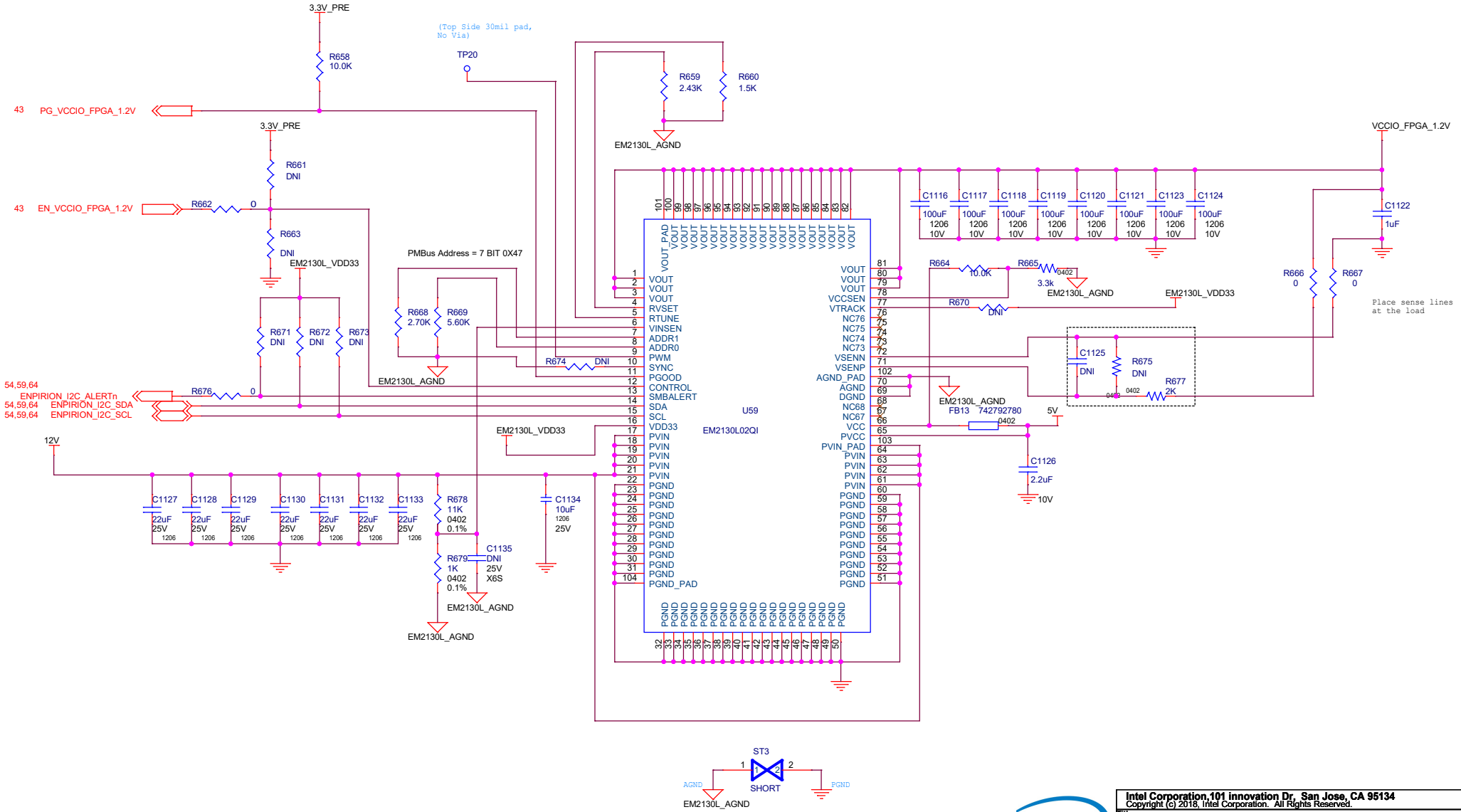
PWR - FPGA VCCIO 1.2V



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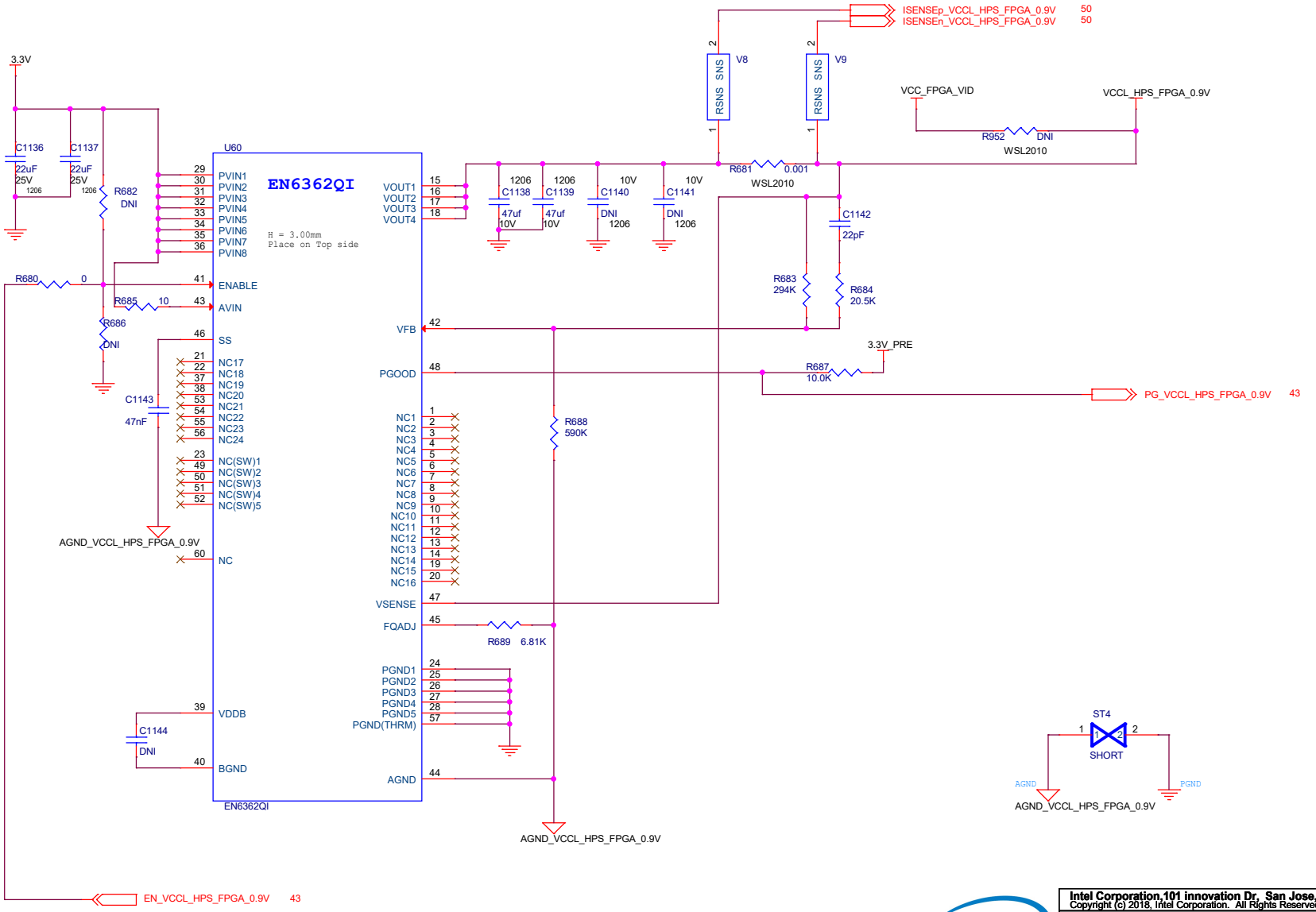
PWR - FPGA VCCL_HPS 0.9V



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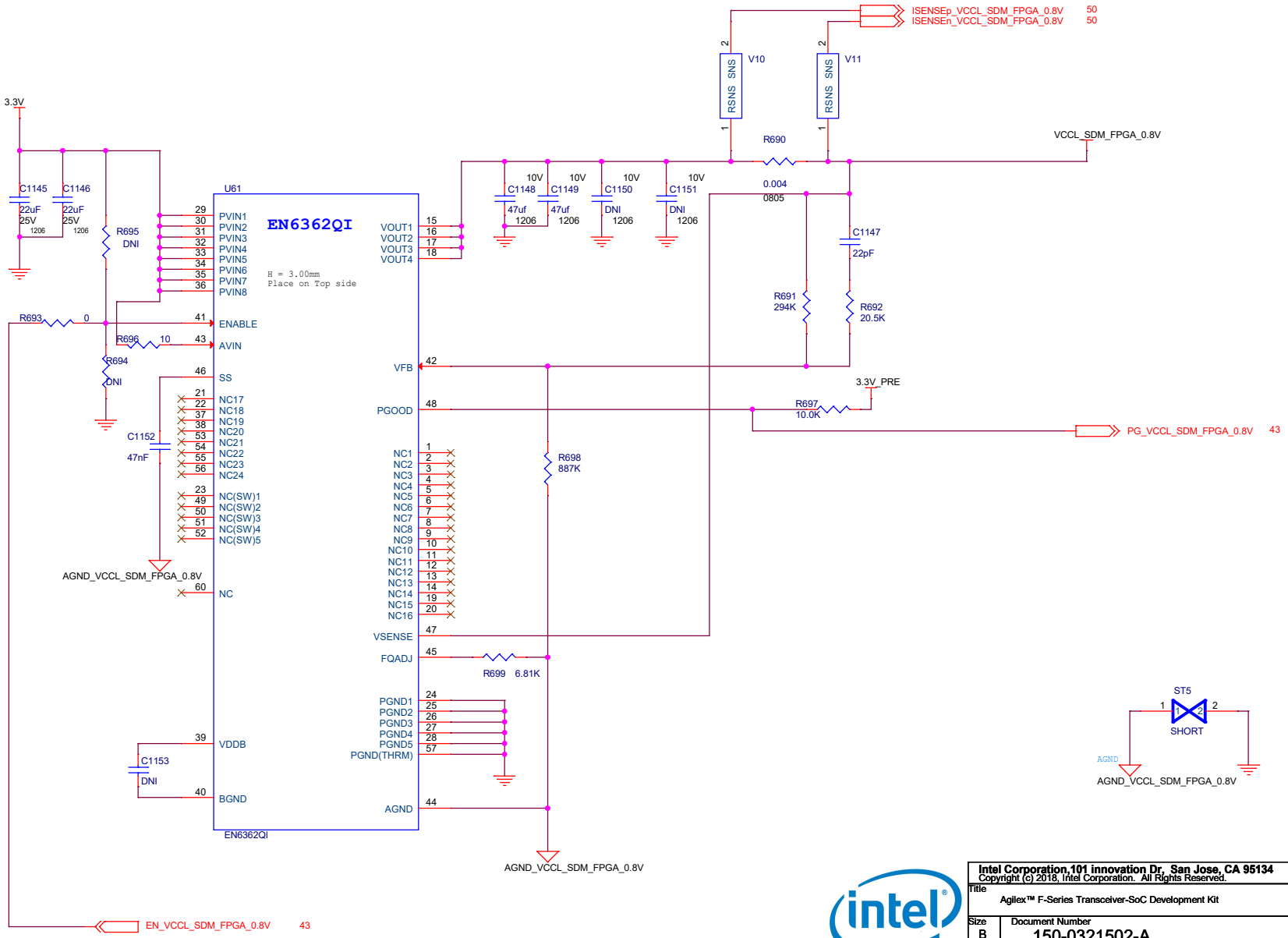
PWR - FPGA VCCL_SDM 0.8V



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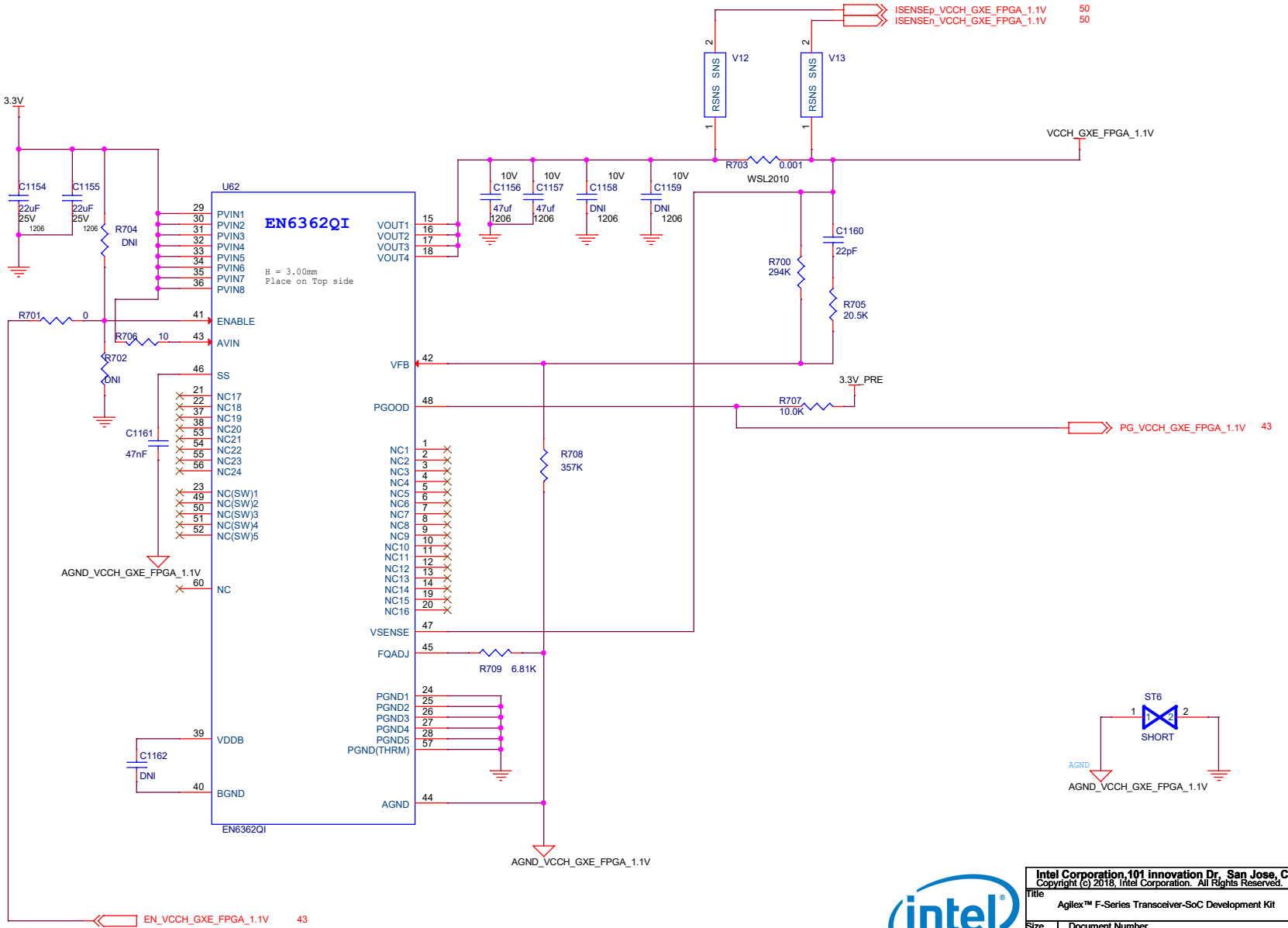
PWR - FPGA VCCH_GXE 1.1V



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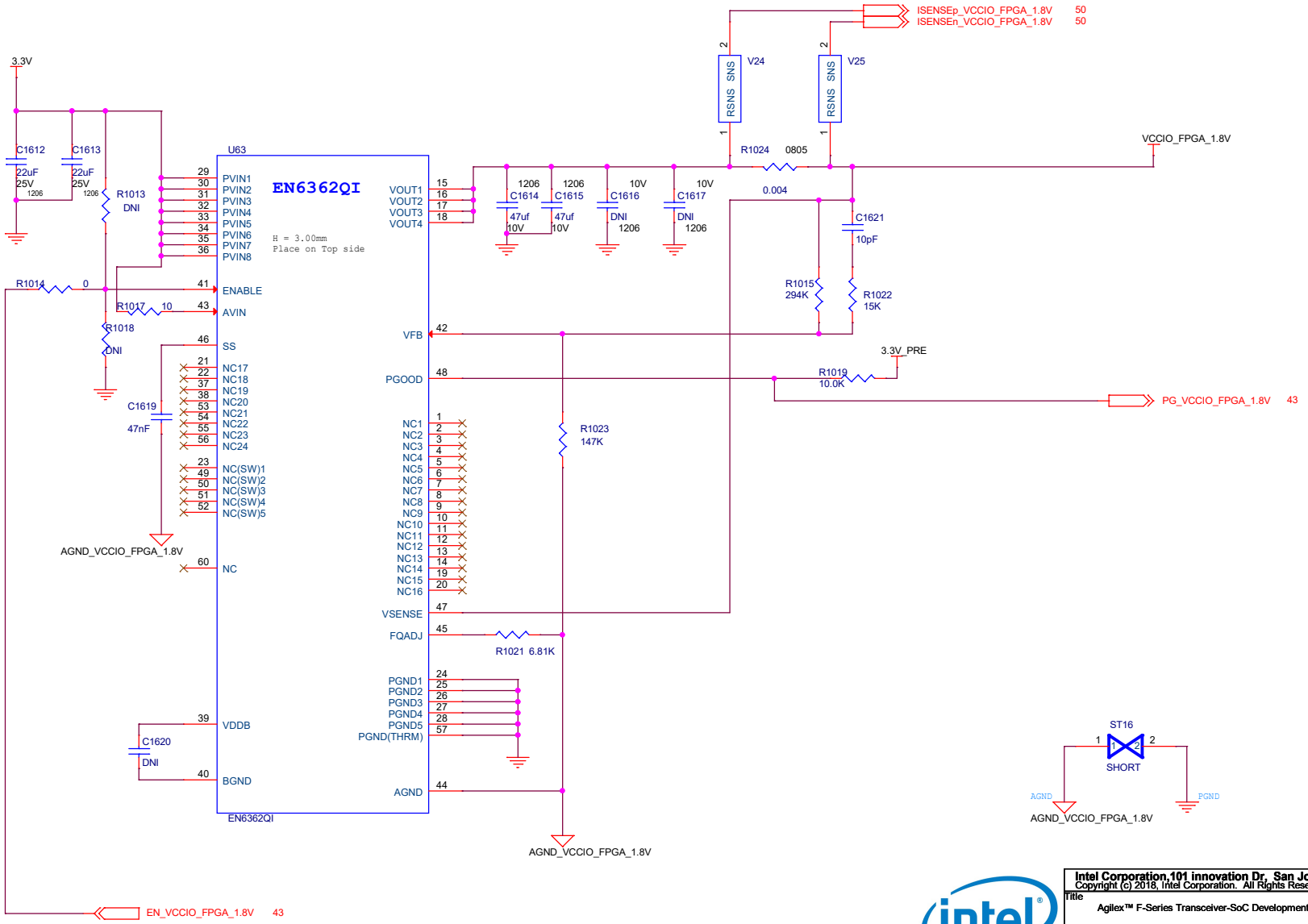
PWR - FPGA VCCIO 1.8V



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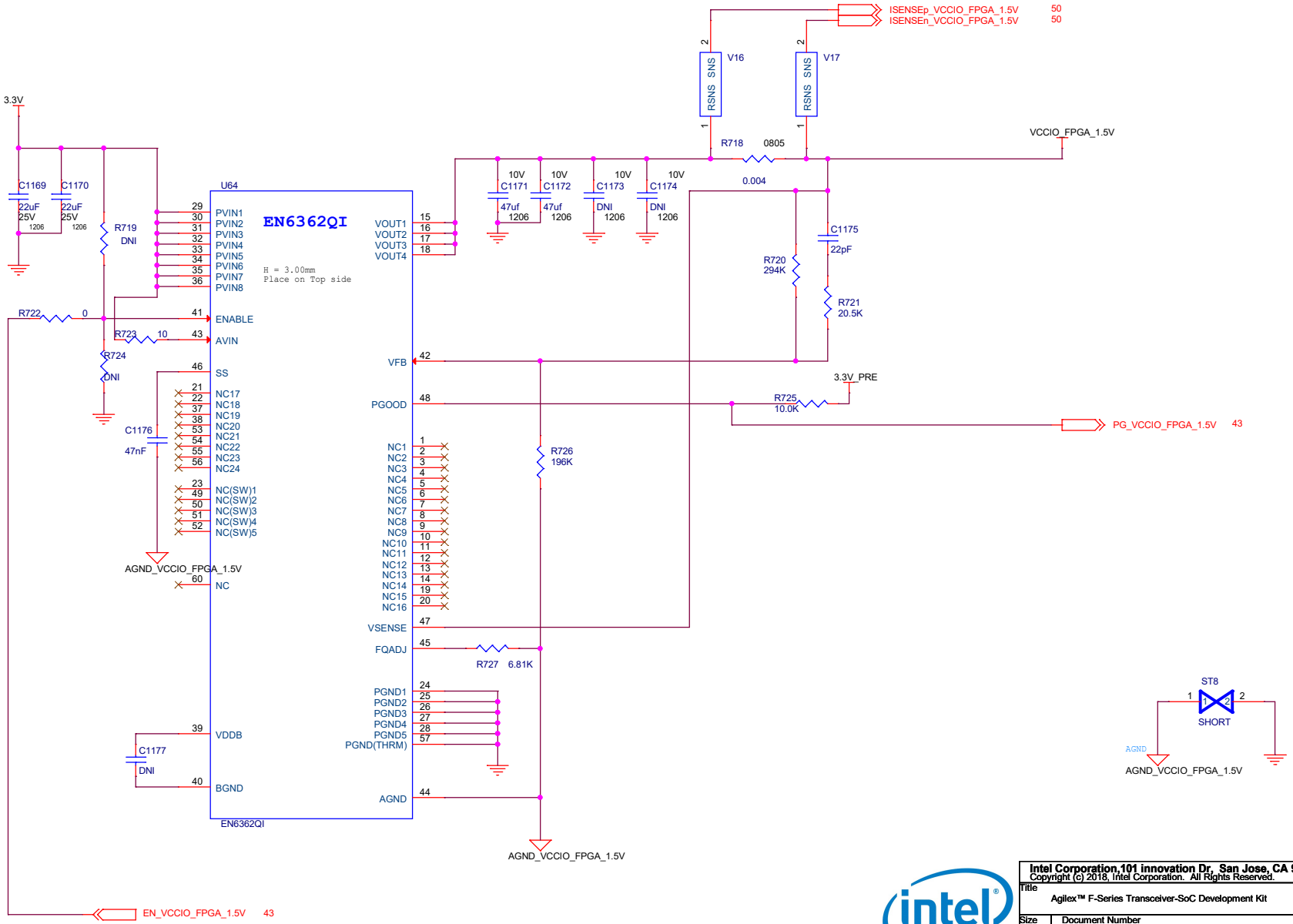
PWR - FPGA VCCIO 1.5V



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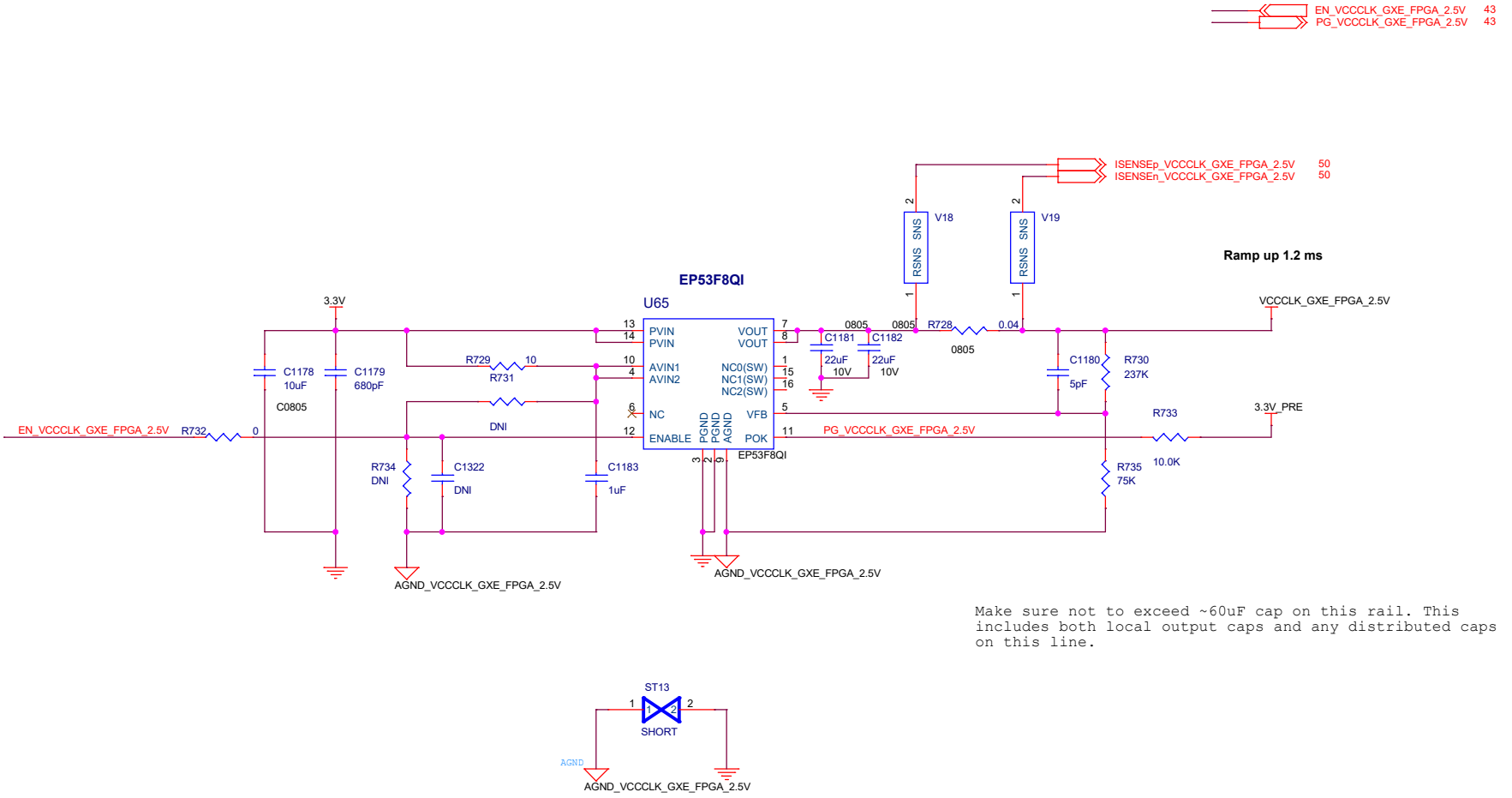
PWR - FPGA VCCCLK_GXE 2.5V



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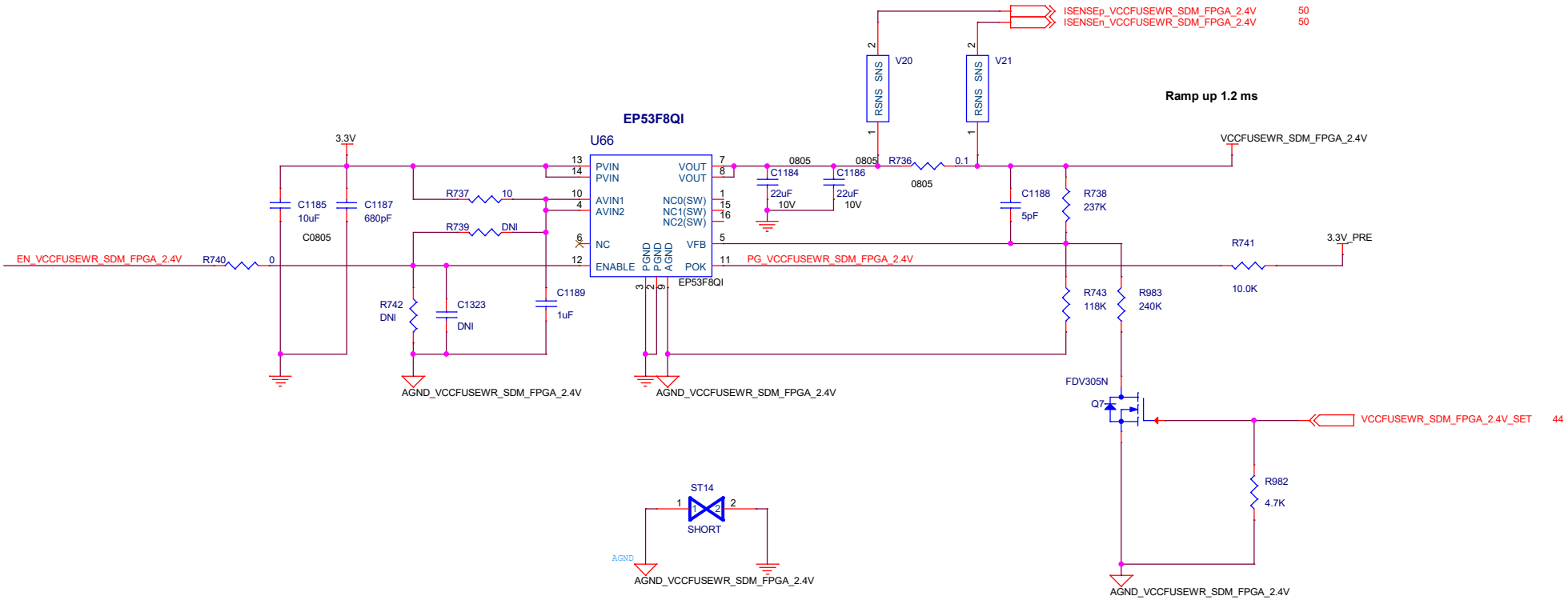
PWR - FPGA VCCFUSEWR_SDM 2.4V

EN_VCCFUSEWR_SDM_FPGA_2.4V 43
PG_VCCFUSEWR_SDM_FPGA_2.4V 43

Make sure not to exceed ~60uF cap on this rail. This includes both local output caps and any distributed caps on this line.



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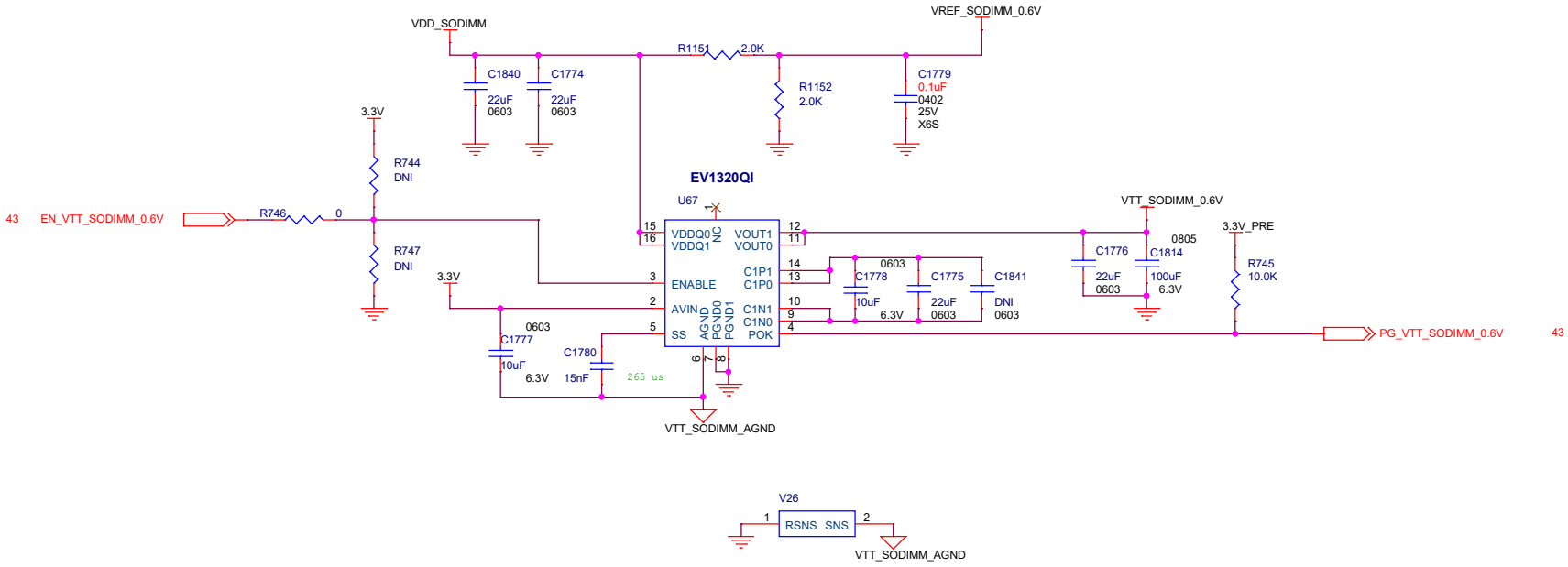
PWR - SODIMM VTT 0.6V



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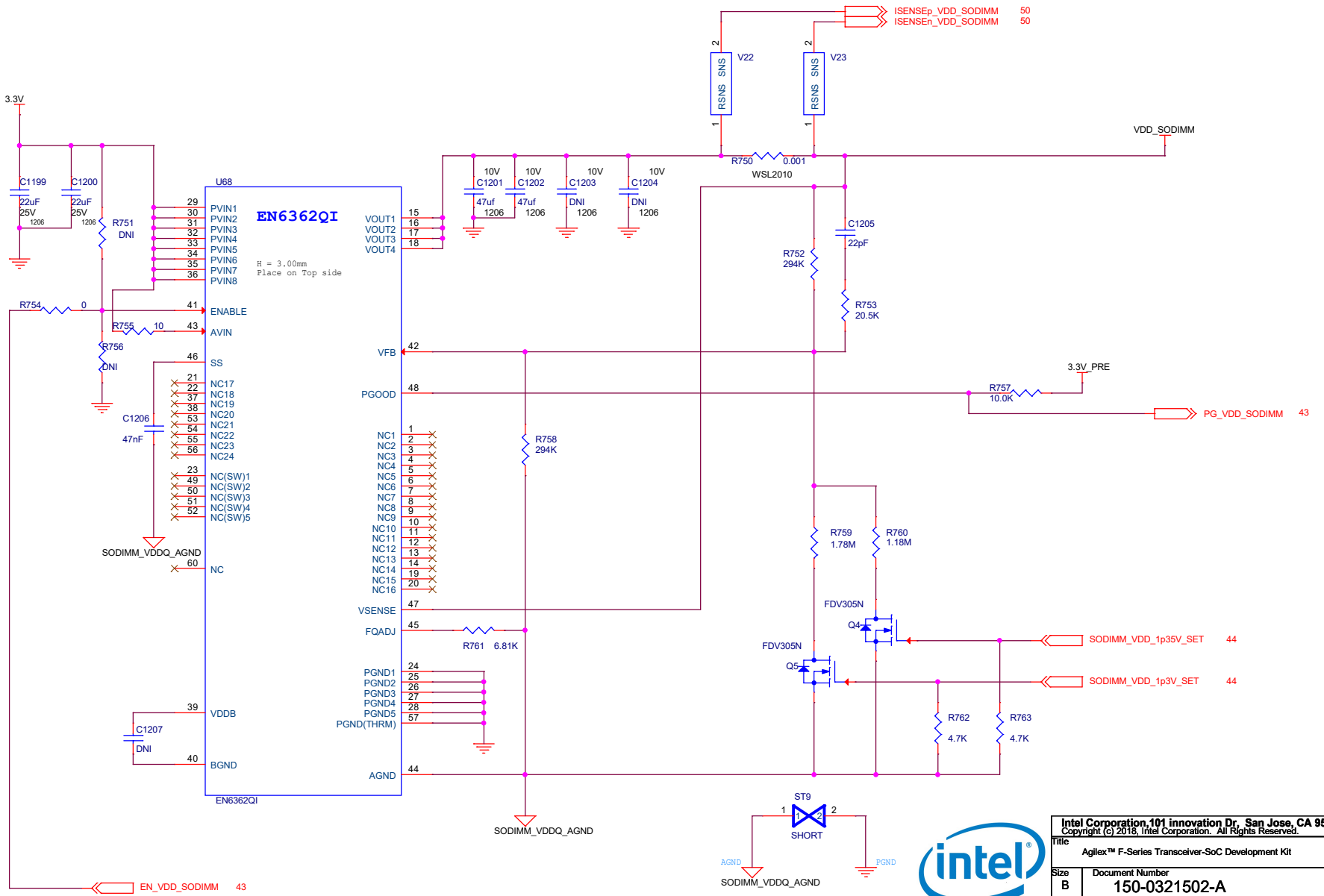
PWR - SODIMM VDD 1.2V-1.35V



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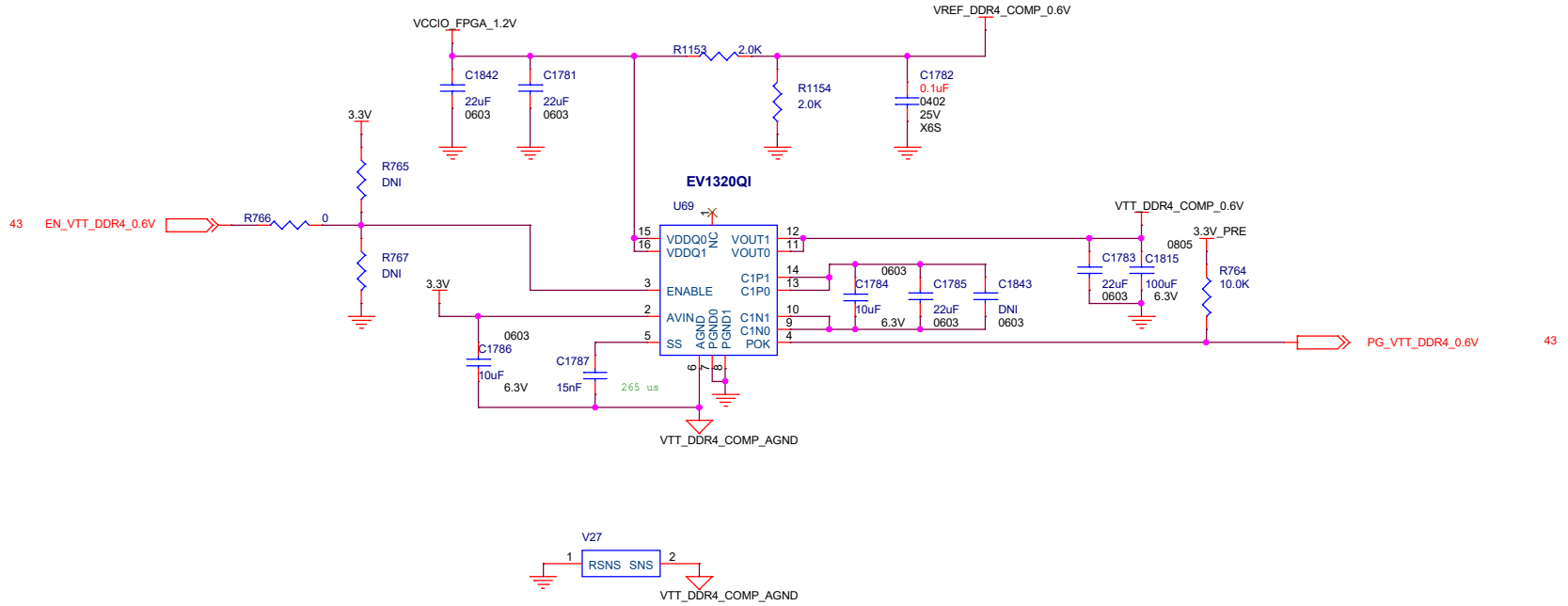
PWR - DDR4 VTT 0.6V



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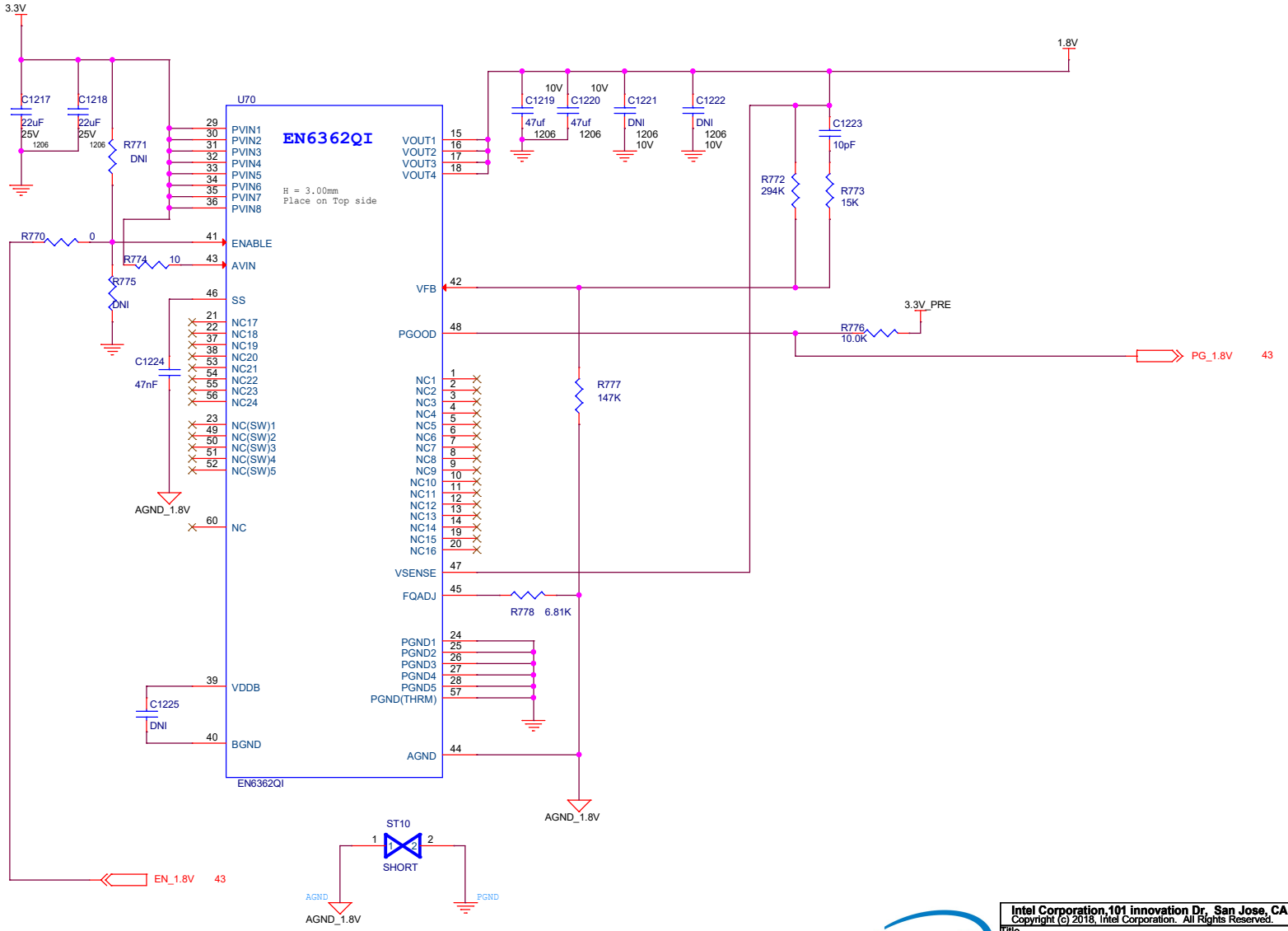
PWR - 1.8V



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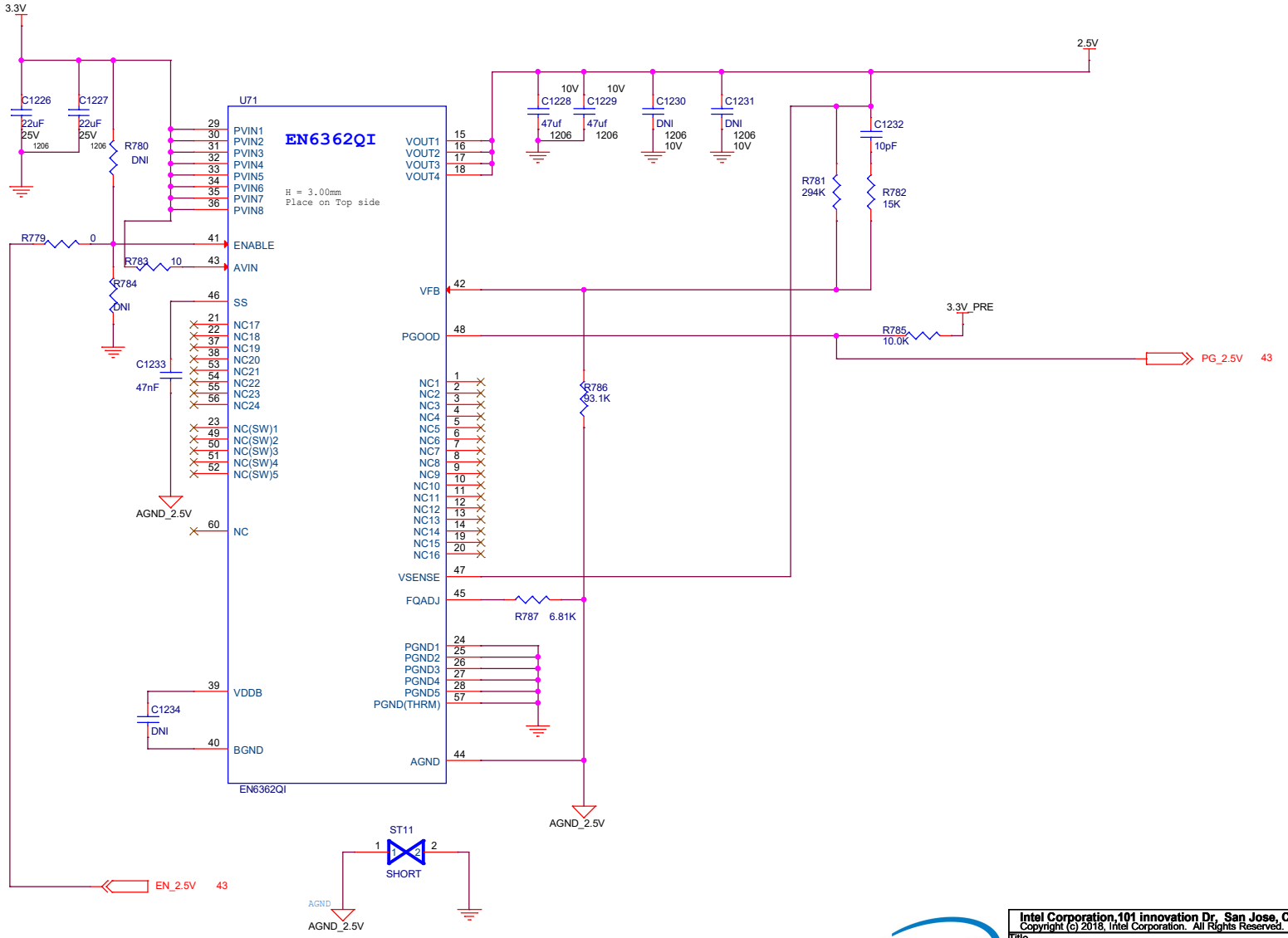
PWR - 2.5V



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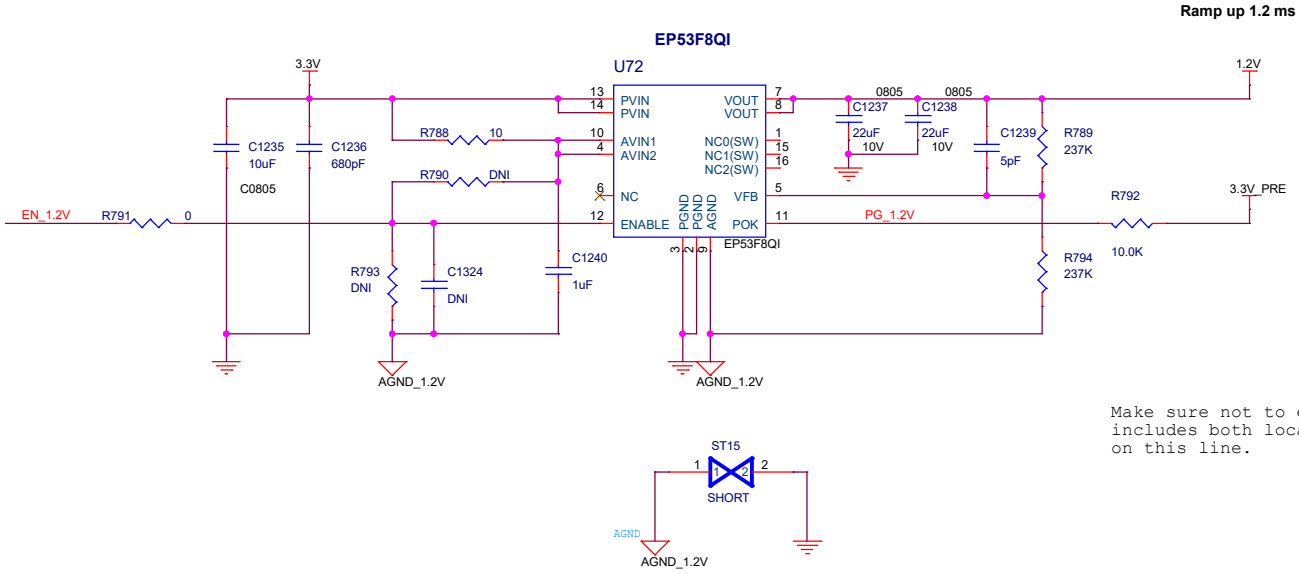
PWR - 1.2V

EN_1.2V 43
PG_1.2V 43



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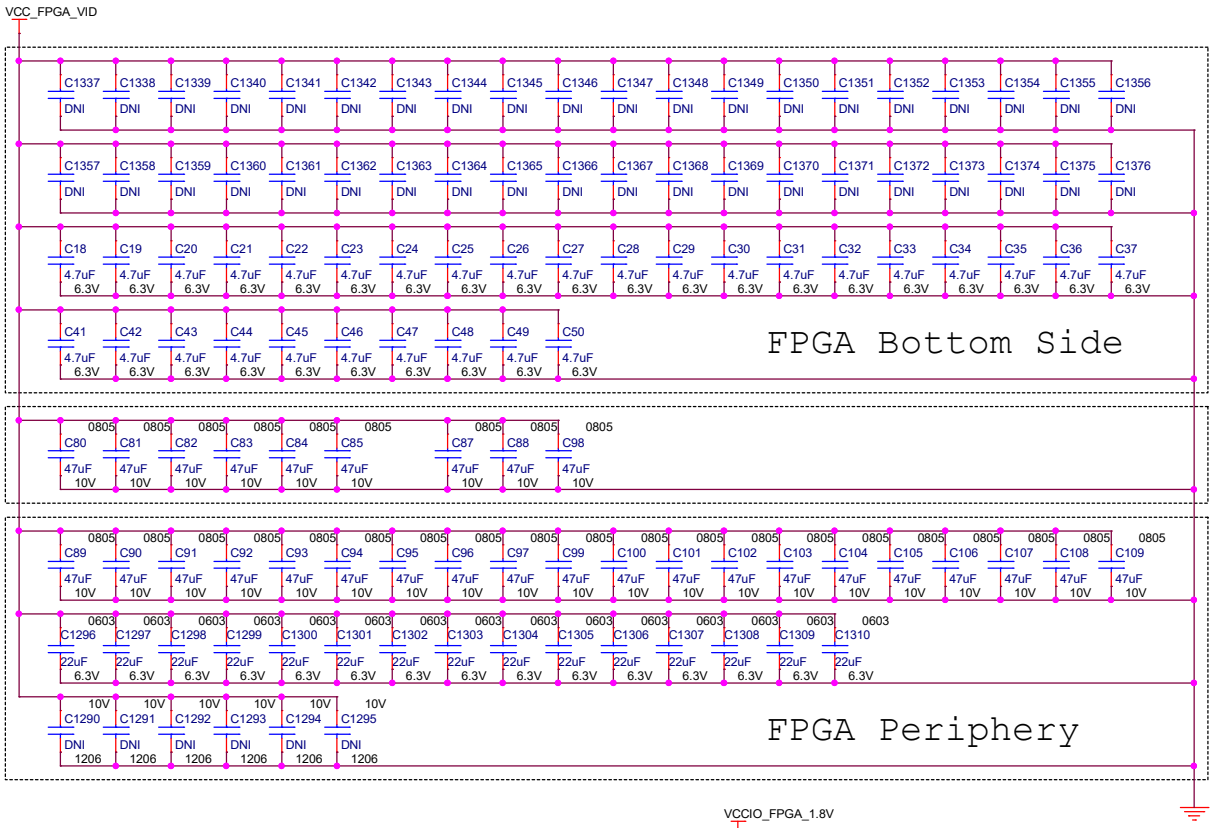
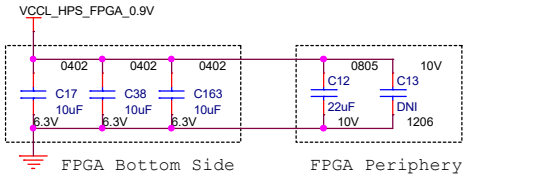
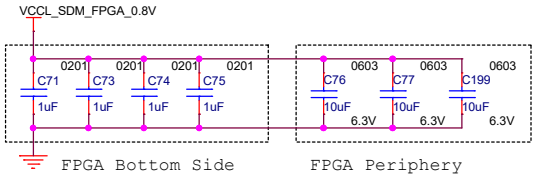
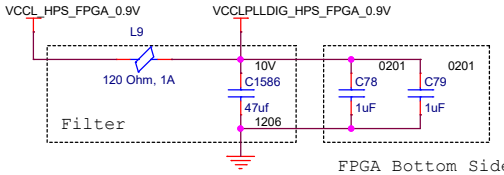
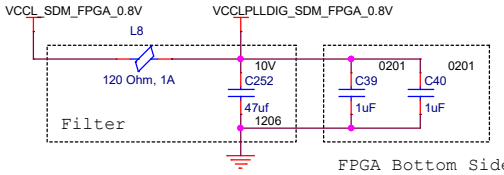
FPGA Decoupling 1



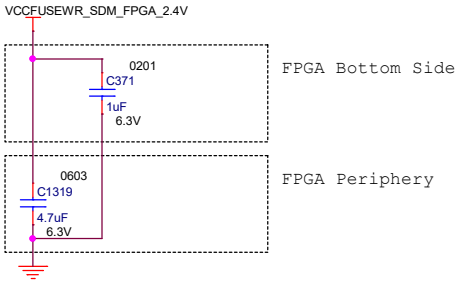


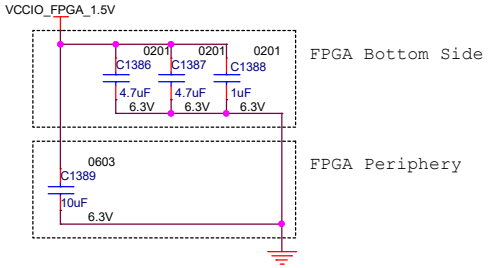


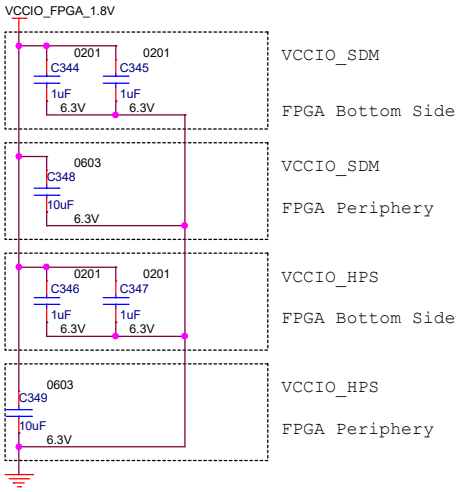




FPGA Bottom Cavity







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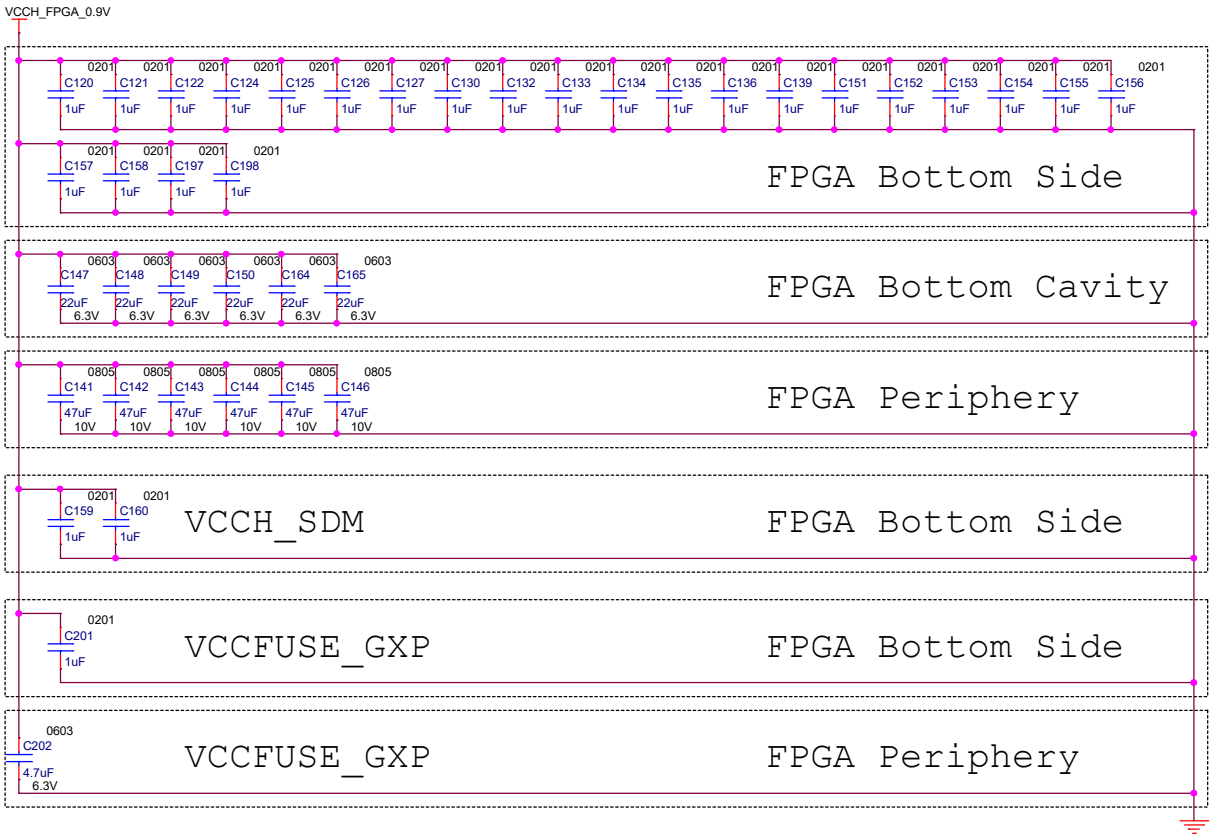
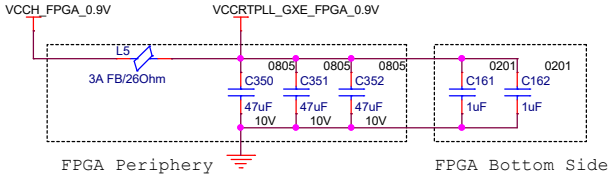
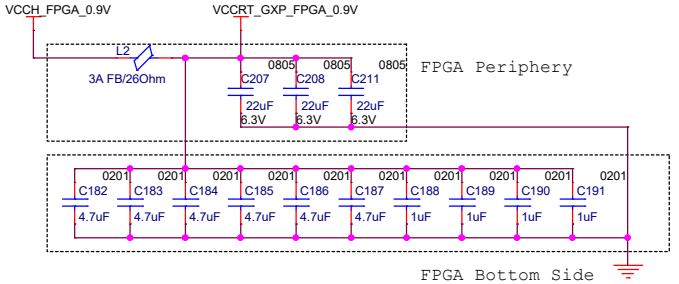
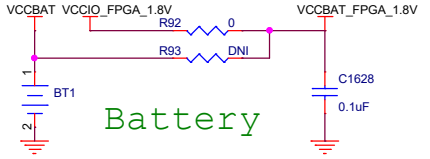
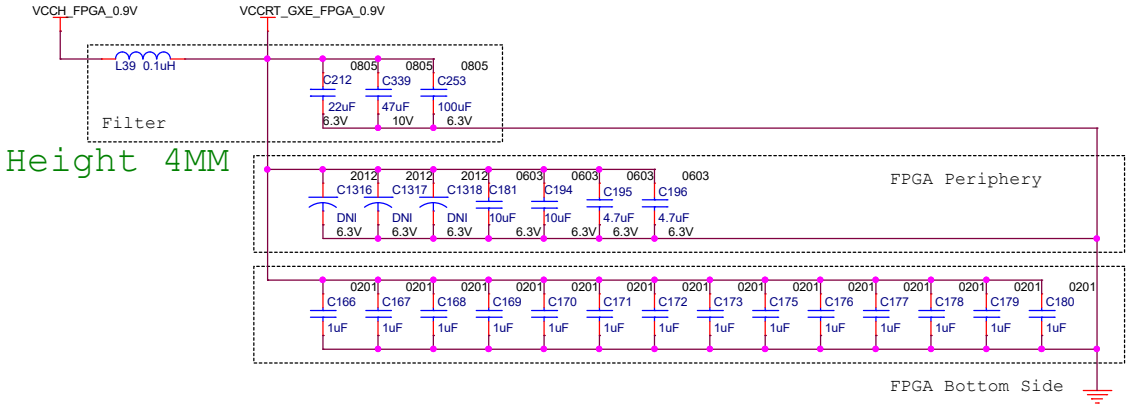
FPGA Decoupling 2

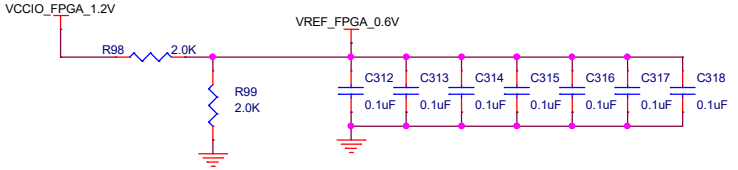












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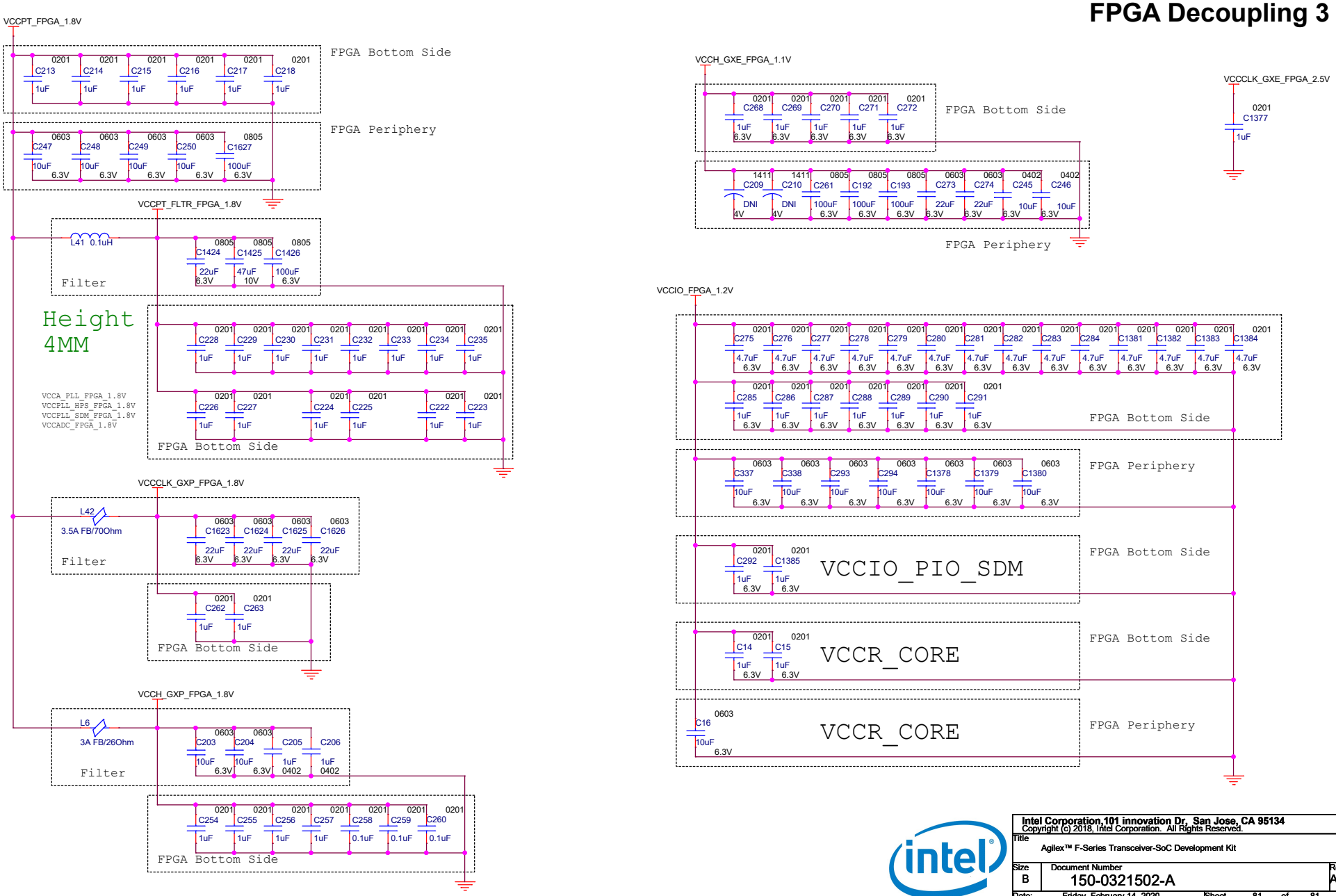
FPGA Decoupling 3



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