Quartus II Software Release Notes

May 2009 RN-01046-1.0

This document provides late-breaking information about the following areas of this version of the Altera® Quartus®II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **\altera\<*version number*>\quartus** directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the Quartus II Device Support Release Notes on the Altera website at **http://www.altera.com/literature/lit-qts.jsp**.

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New Features & Enhancements

The Quartus II software version 9.0 includes the following new features and enhancements:

- The Tasks window, which provides flow-based access to processes and tools available in the Quartus II software, now offers customizable flows based on the two standard flows.
- The Quartus II software version 9.0 provides the SSN Analyzer for improved signal integrity and faster board design. For each input and output pin in the design, the SSN Analyzer estimates the voltage noise caused by simultaneous switching of output pins on the device. The SSN Analyzer is available for the Stratix III device family.
- The new Archiver now allows you to either select pre-defined file sets or create custom file sets for archiving.
- SOPC Builder contains enhanced display filtering features that are useful for large system visualization.
- Advance support for these Arria II GX devices: EP2AGX20, EP2AGX30, EP2AGX45, EP2AGX65, EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260.

- Advance support for these Stratix IV devices: EP4SE230, EP4SE530, and EP4SGX180. In the Quartus II software version 9.0 SP1, advance support for these Stratix IV devices: EP4SGX70, EP4SGX110, EP4SGX230, EP4SGX290, EP4SGX360, EP4SGX530.
- Initial support for these Stratix IV devices: EP4S40G2, EP4S40G5, EP4S100G2, and EP4S100G5.

EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

Synthesis Tools	Version	NativeLink Support
Synopsys Synplify & Synplify Pro	C-2009.03	✓
Mentor Graphics Precision RTL Synthesis	2009a update 1	✓
Mentor Graphics LeonardoSpectrum	2008b	✓
Synopsys Design Compiler	2004.12-SP4	
Mentor Graphics DK Design Suite	5.0 SP5	✓
Simulation Tools	**Version**	**NativeLink Support**
Mentor Graphics ModelSim	6.4a	✓
Mentor Graphics ModelSim-Altera	6.4a	✓
Mentor Graphics ModelSim-Altera Starter Edition	6.4a	✓
Cadence NC-Sim	6.2 (Linux only)	✓
Synopsys VCS / VCS MX	Y-2006.06-SP1	✓
Aldec Active-HDL	8.1 (Windows only)	✓
Aldec Riviera-PRO	2008.06	✓
Formal Verification Tools (Equivalence Checking)	**Version**	**NativeLink Support**
Cadence Encounter Conformal	7.2	
Chip Level Static Timing Analysis	**Version**	**NativeLink Support**
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	**Version**	**NativeLink Support**
Mentor Graphics TAU	3.5.01	
Board Level Symbol/Pin-out Management	**Version**	**NativeLink Support**
Mentor Graphics I/O Designer	7.4	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 9.0	
The **Preserve Hierarchical Boundaries** logic option is removed from the Quartus II software version 9.0. As a result, the **Optimization Technique** and **Gate-Level Register Retiming** logic options do not work when set on entities, unless the entity is a partition.	Use partitions instead of entities.
Changes to the TimeQuest Timing Analyzer behavior in the Quartus II software version 9.0 include the following: ■ **set_net_delay** now constrains from net (output pin) to net/keeper, not individual edges. ■ **read_sdc** now processes HDL-embedded constraints before reading SDC files. ■ **report_min_pulse_width** now performs pulse-width checks at all nodes in the clock network.	
The GXB Migration Guide Reports and temporary migration flow from Arria GX and Stratix II GX to Arria II GX and Stratix IV GX for customer evaluation are no longer available.	Instead of using the migration flow in the software, use a manual altgx migration.
Version 8.1	
The Quartus II software version 8.1 supports Mentor Graphics ModelSim 6.3g. Mentor Graphics ModelSim-Altera Edition and Web Edition are labeled as 6.3g_p1.	
The Quartus II software version 8.1 automatically adds a clock frequency constraint of 10 MHz for the JTAG TCK clock pin for Cyclone III devices, Stratix III devices, and newer FPGA families.	
Version 8.0 SP1	
Exporting a Memory Initialization File (**.mif** or **.hex**) to a RAM Initialization File (**.rif**) format is no longer supported in Quartus II software versions 8.0 and later.	
Version 7.2	
The **Generate back-annotation data for time closure** option in the **Design Entry/Synthesis** page under **EDA Tool Settings** in the **Settings** dialog box is no longer available.	

Description	Workaround
Constraining cells or routing causes problems for designs ported from the Quartus II software version 7.1 or 7.1 SP1 to the Quartus II software version 7.2, because location assignments to the following block types are incompatible: IOPAD IOIBUF IOOBUF FF DDIOOUTCELL DDIOOECELL PSEUDODIFFOUT CLKCTRL (if specified as X,Y,N instead of as a user string)	To prevent this incompatibility, remove the location assignments and the routing constraints.
For the alt2gxb megafunction, when adaptive equalization is activated for a specific channel, rx_eqctrl writes to that channel do not have any effect.	
In the Quartus II software version 7.2, there is no support for DQSB pins in Arria GX devices, but some Quartus II version 7.2 designs require DQSB pins.	
The Quartus II software no longer supports Synopsys Formality software.	
The Quartus II software no longer supports the Synopsys PrimeTime VHDL software.	Use the PrimeTime Verilog software to perform timing analysis for your design. To generate the PrimeTime Verilog files, select **Verilog** in the Format for output netlist list on the **Timing Analysis** page under **EDA Tool Settings**.
The TimeQuest Timing Analyzer supports clock-as-data analysis in the Quartus II software version 7.2, while previous versions of the Quartus II software did not. This results in the TimeQuest analyzer reporting new timing paths where the start point (from node) of the path is a clock node (the target of a **create_clock** or a **create_generated_clock** command. The Classic Timing Analyzer does not support clock-as-data analysis.	The behavior, which is correct, is documented in "The Quartus II TimeQuest Timing Analyzer" chapter in the *Quartus II Handbook*. You may need to modify your constraints to compensate for the clock-as-data analysis support if new timing violations are listed for your design, and you believe these violations are overly conservative for your design.
The functionality of the earlier TimeQuest SDC File Editor has been merged into the main Quartus II Text Editor. The Constraints menu from the earlier TimeQuest SDC File Editor is now located in the Quartus II Text Editor on the Edit menu on the Insert Constraints submenu.	
Starting in the Quartus II software version 7.0, when you use OC-12 with 155.52 Mhz inclock, the alt2gxb megafunction generates a design with incorrect data rate. The incorrect data rate is double of what you designed.	Starting in the Quartus II software version 7.2, when you use the SONET OC-12 protocol with the input clock frequency of 155.52 Mhz, refclk divider is generated by the alt2gxb megafunction in order to obtain the correct data rate.
The TimeQuest Timing Analyzer now performs multicorner timing analysis by default during full compilation. This behavior can be changed in the **TimeQuest Timing Analyzer** page in the **Settings** dialog box.	
Version 7.1	

Description	Workaround
When using the SignalTap II Logic Analyzer, if you select a signal to be tapped that cannot be found in the netlist, the Quartus II software will give a critical warning and proceed with compilation. This is a change of behavior from version 6.1 in which compilation would stop with an error message.	To remove the warnings, remove nonexistent nodes from the SignalTap II Logic Analyzer. To revert to the behavior of version 6.1 and earlier, you can promote all critical warnings to error messages in the Messages section of the **Options** dialog box.
The altlvds_tx megafunction shows the actual phase shift of the tx_outclock generated instead of the core clock frequency. This change is only a change in the information that is displayed, and does not change the actual implementation.	
PLLs in Stratix II and Cyclone II devices now have a new parameter, `sim_gate_lock_device_behavior`, that is OFF by default. This new parameter uses a fixed, internal value of 7 to simulate the gate lock feature. If the value is set to ON, you can simulate the actual device behavior for gated lock using the parameter value gate_lock_counter, as you could in earlier versions of the Quartus II software.	
The Quartus II software version 7.1 Power Analyzer enhances the accuracy of the maximum static power estimate for Stratix II and Stratix II GX devices. The maximum static power drawn from the VCCPD power supply for Stratix II and Stratix II GX devices utilizing maximum power characteristics increases in the Power Analyzer power estimate by at most 15mW (depending on the device size.)	
The Quartus II software version 7.1 issues the error: `"Error (10621): VHDL Use Clause error at <location>: more than one Use Clause imports a declaration of simple name "<name>" -- none of the declarations are directly visible."` However, the Quartus II software version 7.0 and earlier did not issue the error for the same design. This changed behavior arises when a design imports overloaded subprograms with the same signature from different packages such as `STD_LOGIC_UNSIGNED` and `STD_LOGIC_SIGNED`. Both these packages define binary operations on `STD_LOGIC_VECTOR` arguments. Earlier versions of the software incorrectly favored the first imported declaration.	Remove one of the conflicting Use Clauses. For example, use either `STD_LOGIC_SIGNED` or `STD_LOGIC_UNSIGNED`, but not both.

Description	Workaround

The format for Conversion Setup Files (**.cof**) has changed. The element defined below (in DTD syntax) has been introduced:
`<!ELEMENT hex_block (hex_filename,hex_addressing, hex_offset)>`
`<!ELEMENT hex_filename (#PCDATA)>`
`<!ELEMENT hex_addressing (#PCDATA)>`
`<!—hex_addressing value is either relative or absolute --> <!ELEMENT hex_offset (#PCDATA)>`
In addition the following elements have been deprecated:
`<!ELEMENT bottom_boot_block (bottom_boot_filename,bottom_ addressing)>`
`<!ELEMENT main_block (main_filename, main_addressing)>`	

Version 6.0	
The TimeQuest Timing Analyzer's **QSF2SDC** conversion utility cannot properly convert all Classic Timing Analyzer timing assignments. The results from the TimeQuest Timing Analyzer may also be different from the Classic Timing Analyzer due to other default behavior differences.	The **QSF2SDC** conversion utility is considered a guide to help reduce the time to switch to the TimeQuest analyzer, and it is not intended to make the TimeQuest analyzer a plug-in replacement for the Quartus II Classic Timing Analyzer. You should review all converted SDC constraints for correctness and completeness. Refer to the “Switching To the TimeQuest Timing Analyzer” chapter in the *Quartus II Handbook* for more information.
Beginning in the 6.0 release, the Quartus II Parallel Flash Loader megafunction (altparallel_flash_loader) erases flash memory blocks before programming them.	No action is required.
Beginning in the 6.0 release, Quartus II integrated synthesis handles bidirectional pins differently. For example if `bidir1` and `bidir2` are declared as `inouts`, the assignment `bidir1 <= bidir2` creates a directional connection in which data flows from `bidir2` to `bidir1`. In the Quartus II software version 5.1 and earlier, a bidirectional connection was created.	If your design requires that data flow in both directions, you must directly connect the bidirectional pins together without using an assignment statement. Assignment statements always produce a unidirectional data flow.
Version 5.1 SP2 and earlier	
The following megafunctions have clear box models that contain assignments that are not stored in the Quartus Settings File (**.qsf**) and are not written out to a Verilog Quartus Mapping File (**.vqm**): altdqs, altdq, altddio_bidir, altddio_out, altddio_input, altlvds_rx, altlvds_tx, altufm_i2c, dcfifo, alt2gxb_reconfig	Do not save your atom netlist file as a Verilog Quartus Mapping file if you are using these megafunctions.

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 9.0 SP1	
When a RAM is inferred under all the following conditions, the synthesized circuit is not guaranteed to be correct: ■ The read from and write to the memory occur in the same always block or process. ■ The always block or process that reads/writes to the memory array is combinational. ■ The write assignment happens before the read. ■ The RAM is single-port.	To solve this problem, either disable RAM inference or rewrite the HDL description of the RAM. RAM inference can be disabled by setting the ramstyle attribute to "logic" or by setting the `auto_ram_recognition` variable to Off. Alternatively, a different HDL description can be used for the RAM (refer to the "Inferring Memory Functions from HDL Code" chapter in the *Quartus II Handbook*).
When you compile a project, and then try to open the Assignment Editor, the Quartus II software displays an internal error if the selected devices in the **Migration Devices** dialog box include EP4SGX290KF40C3, EP4SGX360KF40C3, and EP4SGX530KH40C3.	In the **Device** page in the **Settings** dialog box, click **Migration Devices**. In the **Migration Devices** dialog box, click **OK** to close the dialog box. In the **Device** page, click **OK** to close the page.

An internal error occurs when you use Incremental SignalTap II to tap an output port that is stuck at VCC or GND.
`Internal Error: Sub-system: AMERGE, File: /quartus/atm/amerge/amerge_incr_tap.cpp, Line: 6076`
`oterm`
`Stack Trace:`
`0x19F1C : amerge_mini_merge + 0x16B3C (atm_amerge)`
`End-trace`
	Remove the tap node from your SignalTap II instance.

In projects targetting Stratix IV GT and Arria GX devices, transceivers with ALTGX instances created in the Quartus II software version 9.0 SP1 might display an internal error in versions of the Quartus II software later than 9.0 SP1:
`Internal Error: Sub-system: FHSSI, File: /quartus/fitter/fhssi/fhssi_cell_group.cpp, Line: 1463`
`aux_cell != NULL`
	Regenerate the ALTGX instances.

Version 9.0	

Issue	Workaround
In the Quartus II software version 9.0, the **set_net_delay** Tcl command is optimized by the Fitter, but in the Quartus II software version 8.1, it was not.	The Quartus II software version 9.0 correctly optimizes this command in the Fitter. Re-run the Fitter on your design in the Quartus II software version 9.0.
The Quartus II software version 8.1 did not correctly synthesize case statements if the case expression is smaller than the case item expressions and contained a binary or ternary operator, for example (address << 2).	The incorrect synthesis is fixed in the Quartus II software version 9.0. To avoid the issue when compiling with the Quartus II software version 8.1, increase the size of the case expression. You can do this artificially by adding *<N>*'sb0 to the expression, where *<N>* is the size of the largest case item expression.
The ALTGX MegaWizard allows the reset ports to be selected or deselected. But deselecting the reset ports may make the simulation output become undefined.	Always keep the reset ports enabled.
If you use the Advanced I/O Timing feature and migrate from the Quartus II software version 8.1 or earlier, you may see decreased minimum pulse width requirements on the I/Os compared to the previous versions. This can result in increased f_{MAX} on some paths. The change only applies only to I/O pins with board trace models that include transmission lines.	
In the Quartus II software versions 9.0 and later, STRATIX_II_TERMINATION assignments are ignored for Cyclone III, Stratix III, and Stratix IV.	In the Quartus II software version 9.0, these assignments are ignored. Use the **Input Termination** and **Output Termination** logic options to make on-chip termination (OCT) assignments in Cyclone III, Stratix III, and Stratix IV device families. Check the Fitter report panels after fitting to verify which OCT value is applied to each pin.
When a design targeting the Arria II GX or Stratix IV families is simulated in the Quartus II software, the `rx_bistdone` output signal of the altgx megafunction does not go high in PRBS high, low, or mixed frequency settings. This behavior is expected hardware behavior, and the data pattern generated is for PMA signal observation.	Ignore `rx_bistdone` and `rx_bisterr` in these settings.
In the ALTGX MegaWizard, the GT Common Mode Voltage is 1.2V, but the MegaWizard shows 1.1V.	The Quartus II software ignores the incorrect voltage.
During simulation in the Quartus II software version 9.0, the output busy signal becomes stuck in an undefined state even if any of the inputs to the altgx_reconfig block are correctly set as undefined.	Add a reset port.
Designs targeting Stratix IV devices and that contain instances of the altgxb megafunction may take more than an hour in Analysis & Elaboration or Analysis & Synthesis.	
To use the OpenCore Plus hardware evaluation feature with unlicensed IP that supports the feature, you must first select a specific device. The Quartus II software version 9.0 and later does not support the OpenCore Plus hardware evaluation feature for Auto devices.	On the **Device** page in the **Settings** dialog box, turn on **Specific device selected in 'Available devices' list** and select a specific device in the **Available devices** list.

Issue	Workaround
The following Internal Error in the Quartus II software version 9.0 occurs because RAMs with one word are not allowed in the Quartus II software version 9.0. `Internal Error: Sub-system: ASMRAM, File: /quartus/comp/asmram/asm_ram_model_base.cpp`	Update the design to remove the one-word RAM. If the affected design contains DSP logic generated with DSP Builder, re-generate the DSP logic with DSP Builder version 9.0.
When you select an item in the **Data Transfer FIFO Depth** list in the Scatter-Gather DMA Controller MegaWizard, the selection has no effect because the actual FIFO depth is a value calculated from a fixed formula.	In the Quartus II software version 9.0, keep the default and do not change the selection in the **Data Transfer FIFO Depth** list.
In the Quartus II software version 9.0, when P**erform Physical Synthesis for Combinational Logic for Performance**, formal verification cannot be used for 45nm and 65nm device families. When setting the formal verification tool, you may see an error.	

If the design uses the altgx megafunction and dynamic reconfiguration with an alternate Transmitter PLL, there is a problem when the alternate transmitter PLL logical reference index is 0. The issue could occur when placing two channels in the same quad, and each channel then starts up using different PLLs. The problem you see is the following internal error during Analysis & Synthesis:
`Internal Error: Sub-system: DSTR, File: /quartus/h/dstr_translator_auto.cpp, Line: 1773`
`The calling function has passed an illegal DEV_PART_ENUM`
`Stack Trace:`
`0x9BE8 : DSTR_TRANSLATOR::get_user_string + 0x28 (DDB_DSTR)`
`0x1900 : dstr_get_user_string + 0x10 (DDB_DSTR)`
`0x36DA02 : cut_get_clock_divider_cdb_atom_tgx_hssi_clock_divider_enum_tgx_hssi_pll_base_data_rate_tgx_hssi_config_atom_nodes + 0x153F2 (db_cut)`
	Specify the base data rate on the first page of the MegaWizard.

The following input clock frequencies are invalid for SONET OC12, but show up in the ALTGX MegaWizard: ■ 124.416 MHz ■ 248.832 MHz ■ 497.664 MHz	Choose only one of the following input clock frequencies: ■ 311.04 MHz ■ 77.76 MHz ■ 62.208 MHz ■ 622.08 MHz ■ 155.52 MHz

Issue	Workaround
When you click **Open Options dialog box - Text Editor page** in the "Use an External Text Editor" page in the Tips & Tricks in the Quartus II software, the **Printing** page in the **Options** dialog box opens.	In the **Category** list, click **Text Editor** in the **Options** dialog box.
When you use the CMU PLL, the ALTGX MegaWizard does not allow you to disable the central clock divider option.	Run the following command: **qmegawiz -silent -wiz_override=USE_GLOBAL_CLK_DIVIDER=FALSE** *<design>*
In the Quartus II software version 8.1, clock uncertainty assignments that are automatically applied by **derive_pll_clocks** for soft-CDR was too pessimistic for the rising edge to rising edge and falling edge to falling edge clock transfers of `loaden` signal for hold analysis.	Either run timing analysis in the Quartus II software version 9.0 or manually set the uncertainty value of rising edge to rising edge and falling edge to falling edge clock transfers of the `loaden` signal to 0 for hold analysis.
The ALTGX MegaWizard allows you to choose the ATX PLL for PCIe 2.0 applications; however, this configuration doesn't work properly in 230ES or 530ES silicon.	The ATX PLL placement constraints may be more constrained for some devices, and it's recommended that the pin out is created with the ATX PLL. Once the pin placement is fixed, update the ALTGX instance and choose the CMU PLL for the PCIe 2.0 configurations.
Currently the MegaWizard for the Floating Point Matrix Multiplier megafunction allows you to create a multiplier of 256 or more columns in matrix AA, or rows in matrix BB. However, the actual supported column size of matrix AA or row size of matrix BB must be less than 256, or you will receive an unexpected result.	
If you set the value of the base data rate different from the value of the effective data rate, the **pre_divide_by** on the ***<family name>*_hssi_clock_divider** is incorrect.	Manually update the value to the required value so that the value of **base_data_rate**for **pre_divide_by** is the same as the value for **effective_data_rate**.
Version 8.1	
In the Quartus II software version 8.1 and later, the Tcl **project_open** and **set_current_revision** commands no longer overwrite the compilation database when the database version is incompatible with the current version of Quartus II software. Instead, they generate an error.	To avoid the error and overwrite the database, run `project_open -force` or `set_current_revision -force`.
The Assignment Editor does not allow you to edit the location assignment of the GXB Central control unit.	Modify the assignment manually in the Quartus II Settings File (**.qsf**) while the project is closed.
When LVDS transmitter is implemented using logic cells and when you select **Odd deserialization factor**, the MegaWizard allows you to choose between the `tx_inclock` and `tx_coreclock` port to register the `tx_in` port. However, it is incorrect to register `tx_in` using the `tx_coreclock`. This issue does not affect LVDS implementations using the hard SERDES or any implementation using even deserialization factors.	Either preregister the `tx_in` using a clock with frequency of (`output_data_rate/deserialization_factor`), or supply a clock of this frequency to the LVDS via the `tx_inclock` input port and use that clock to register the `tx_in` inputs.
The timing constraints auto-generated by the Quartus II software for the `altlvds rx_divfwdclk` output (that is, when in Soft-CDR mode) were incorrect in versions of the Quartus II software earlier than 8.1. The constraints did not correctly account for an inversion in the `rx_divfwdclk` clock path.	This issue has been resolved in the Quartus II software version 8.1. Modify designs using a Synopsys Design Constraints File (**.sdc**) with `rx_divfwdclk` timing constraints generated by a version of the Quartus II TimeQuest Timing Analyzer earlier than 8.1 to use the correct timing constraints (as generated with the current version of the TimeQuest analyzer).

Issue	Workaround
The **Enable** column in the Pin Planner shows only location assignments, and does not show whether other types of assignments are disabled or enabled.	Use the Assignment Editor to view and disable assignments.
Version 8.0	
If you compile a project in the command line, and you open the Quartus II software GUI on that project, you may experience unexpected and/or incorrect results.	While compiling a project in the command line, do not open the Quartus II software GUI on that project.
The **Open** dialog box does not display all files.	Restart the Quartus II software to see all the files.
Creating a new project from the TimeQuest Timing Analyzer GUI can crash the TimeQuest analyzer GUI.	Because the TimeQuest analyzer GUI depends on the open project in the main Quartus II software GUI, create or change projects in the main Quartus II software GUI and not the TimeQuest analyzer GUI.
The following error occurs when you manually connected the `seriesterminationcontrol` and `parallelterminationcontrol` ports on an output buffer atom, but did not make a termination assignment to the corresponding I/O that uses calibrated on-chip termination: `"Output buffer atom <name> has port <name> connected, but does not use calibrated on-chip termination"`	Disconnect the `seriesterminationcontrol` and `parallelterminationcontrol` ports on the specified output buffer atom, or make an **Input Termination** or **Output Termination** assignment to the corresponding pin that uses a value that includes **With Calibration**.
When you connect the dynamic termination control port on the output buffer of a dedicated output I/O, the error `"Output I/O <`*name*`> has dynamic termination control connected"` occurs in a design with no previous errors.	If the I/O was generated as part of an IP block, regenerate the IP block. If the I/O was user generated, then disconnect the `dynamicterminationcontrol` port, or connect it to `0` or logical ground.
An error is issued saying that an output is inverted when feeding the `dynamicterminationcontrol` port of an output buffer atom.	Remove the specified inversion.
If there are **Dynamic Termination Control Group** assignments to two different I/Os in the design that have different dynamic termination controls but are assigned to the same group, you will receive the following error: `"Atoms <name> and <name> are assigned to the same dynamic termination control group, but their dynamic termination controls are not compatible"`	Remove all **Dynamic Termination Control Group** assignments from the design, because they are no longer necessary. If the assignments were created by an IP block, regenerate the block.
The Merged Registers and the Inverter Push-Back Through Register report panels under the Analysis & Synthesis Formal Verification report may be missing or incomplete in the Quartus II software versions 8.0 and later.	The information is available in the following two report panels in the Analysis & Synthesis Optimization Results report under Register Statistics: Registers Removed During Synthesis (for merged registers), and Inverted Register Statistics (for inverted registers)

Issue	Workaround
In the Quartus II software versions 8.0 and later, I/O primitives do not support exact pin location assignments for designs targeting Cyclone III, Stratix III, and Stratix IV devices. If your design contains I/O primitives with exact pin location assignments, you will see the following error: `The location assignment on the I/O Primitive instance "inst1" specifies an exact pin location`	Instead of using an I/O primitive you can set an exact location using the `chip_pin` attribute, or through the Assignment Editor.
Projects created in versions of the Quartus II software earlier than version 8.0 that use Incremental Compilation will not work properly with the smart compilation feature in the Quartus II software versions 8.0 and later. A message specifying a detected change in the `partition_hierarchy` assignment is issued and all stages of the flow are executed. Design Space Explorer, which leverages smart compilation technology, is also affected.	In the Quartus II software versions 8.0 and later, open the project in the GUI and re-save the project before using the Design Space Explorer or smart compilation.
A new assignment check was introduced in Quartus II software version 8.0 that checks whether I/Os are fully constrained. Any I/Os that are not fully constrained appear as a line in a table in the Fitter report under I/O Assignment Analysis Warnings. The reason for the warning appears in the table. Certain conditions are warnings; others are errors. For example, an I/O with no assignments at all will have a reason of "Incomplete set of assignments" and an I/O with only an I/O standard assignment will have a reason of "Missing drive strength and slew rate".	Fully constrain I/Os to remove these warnings.
Version 7.2 SP1	
When reading a Memory Initialization File (**.mif**), Quartus II software versions 7.2 and later generate “uninitialized memory addresses” messages, such as: Warning: 2 out of 32 addresses uninitialized. Initializing them to “0”. 2 warnings found. Warning: Address 1 is not initialized. Warning: Address 3 is not initialized. Quartus II software versions earlier than version 7.2 do not have this issue.	Open the affected Memory Initialization File and search for the “%” character. Because the Quartus II software version 7.2 supports multiline commenting beginning with a “%” and ending with a “%”, if the “%” character is found in the Memory Initialization File, ensure that it does not act as a multiline separator that treats the address data as a comment, or remove the “% in the Memory Initialization File.
Version 7.2	
Live I/O check may produce an error if reserved pin directions are changed while live I/O check is enabled.	Turn live I/O check off and back on again to remove the error.

Issue	Workaround
Using Parallel Flash Loader IP optimized for speed adversely affects the CFI device programming time when using the EthernetBlaster download cable.	Use the USB Blaster or ByteBlaster II download cable instead of the EthernetBlaster Download Cable, or use the Parallel Flash Loader IP optimized for area instead of speed.
Version 7.1	
On Windows, the following cores may fail to run when the `PERL5LIB` environment variable is set: 8B10B Encoder-Decoder POS-PHY Level 4 RapidIO SerialLite II	Delete the `PERL5LIB` environment variable: Right-click My Computer and click **Properties**. Click the **Advanced** tab, and then click **Environment Variables**. Delete **PERL5LIB** under both **User variables** and **System variables**. Restart the Quartus II software.
The Quartus II software can reduce RAM by modifying control signals while maintaining functionality. For example, in many cases a read enable can be converted into a clock enable.	
If you open the **Print** dialog box or the **Page Setup** dialog box in the Quartus II software, and if you use an HP Business Inkjet 1200 series printer, the Quartus II software may produce an unexpected error.	If you have this printer, Altera recommends updating to the latest version of the drivers, available for free download from the HP website.
Altera recommends that all soft-CDR channels driven by a PLL are within a distance of 25 SERDES rows (including the unbonded SERDES) from that PLL.	
When you launch documentation (PDF and HTML files) from the MegaWizard Plug-In Manager, the MegaWizard uses the **Web browser** option in the **Internet Connectivity** page of the Quartus II **Options** dialog box. The MegaWizard will sometimes use a setting from a previous version of the Quartus II software than the present version. This can lead to errors if the web browser does not exist on your machine.	Manually edit the `WEB_BROWSER` variable in the **quartus2.ini** file and remove the reference to the non-existent web browser.
Version 6.1	
You may get one or more messages `"Error: Can't generate programming files for project because design file "<name>" is encrypted. It does not have license file support that allows generation of programming files"` from the Assembler when compiling a design that is using Altera IP with the OpenCore Plus evaluation feature when your design has VHDL source files that have the construct `"use work.all;"`.	The errors are reported for IP source files that were added to your project by IP Toolbench, but which are not actually used during compilation. Remove the files listed in the error messages from your project file list and recompile the design.
When a design contains IP that is evaluated using the OpenCore Plus hardware evaluation feature, the Quartus II software produces a sequence of Info messages beginning with `Info: Elaborated megafunction instantiation "pzdyqx:nabboc"`.	These messages can be safely ignored.
Version 6.0 SP1	

Issue	Workaround
Running multiple instances of the Quartus II software using the same Quartus Project File (**.qpf**) may cause unpredictable results or may cause the Quartus II software to crash.	Altera recommends that you not open multiple instances of the Quartus II software using the same project.
Version 6.0	
In the classic Timing Analyzer, when a clock (base or derived) is assigned to an internal register, then data paths to and from the register are not analyzed for clock setup and clock hold analysis.	First, analyze the design with the clock settings assigned to the internal registers. Then remove the clock settings from the internal registers and perform a second analysis, checking only paths to and from those registers. The other resolution is to use the TimeQuest Timing Analyzer instead of the classic Timing Analyzer.
The TimeQuest Timing Analyzer erroneously analyzes paths to the asynchronous data pins of registers (that is, the `adata` pin) during a recovery/removal analysis.	Apply the `set_false_path` command from the asynchronous data signal's source port or register to declare these paths as false paths.
If you change the type of a parameter setting in the Quartus II Settings File (**.qsf**) or a Block Design File (**.bdf**) and recompile your design, your change appears to have no effect. The type of a parameter is denoted by appending a prefix such as "B" (binary), "D" (decimal). For example, B"10101" represents the binary string "10101", but D"10101" represents the decimal number 10101.	Delete the ***<project>*\db** directory and recompile the design.
Version 5.1 SP2 and earlier	
Path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to Windows and Linux platforms.
If you make a single-point `CUT=ON` assignment to a node, and then override it with a point-to-point `CUT=OFF` assignment on a specific path, the `OFF` assignment will not be honored.	
The Classic Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name **file.eda.edif**.	Use design file names with only one extension.
Running individual Quartus II software executables (**quartus_map**, **quartus_fit**, and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	Run individual executables either from within the Quartus II scripting shell (**quartus_sh**) or directly at a command prompt.
Do not open, change permissions, or delete the ***/<project directory>*/db** directory or any file therein while any Quartus II executable is running.	

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 9.0 SP1	
For Windows Vista 64-bit, when you install the update for the Quartus II software version 9.0 SP1, the software requires you to terminate the jtagserver process before you update.	Reboot before installing the Quartus II software version 9.0 SP1, without opening the 9.0 software in between rebooting and installing.
Version 9.0	
When Parallel Synthesis is on, the **Stop** button in the Quartus II software GUI may not stop all the child processes of **quartus_map** in Windows.	Use the Task Manager window to stop all the child processes.
Version 8.0	
The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network, including displaying popups.	To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 (**support.microsoft.com/?kbid=896054**) for more information about possible workarounds.
Version 7.2 SP1	
When you install the Quartus II software version 7.2 SP1, the Nios II IDE, or any Altera-provided patches on Windows Vista with **User Account Control (UAC)** turned on, the Program Compatibility Assistant issues the warning: `"This program might not have installed correctly."`	You can safely ignore this message by selecting **This program installed correctly** or you can turn off UAC before installing the software.
Version 5.1 SP2 and earlier	
If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly, for example: ■ Software guards (parallel and USB) ■ Programming with JTAG server	Altera recommends that you have Administrator privileges when installing the Quartus II software.
If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.	Limit the full, hierarchical instance name to fewer than 247 characters if possible.
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report `"JTAG Server -- internal error code 82 occurred"` when you click the **Add Hardware** button in the **Hardware Setup** dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the **jtagserver.exe** program and at a command prompt for that directory, type `jtagserver --install` <Enter>

Linux Platforms Only

Issue	Workaround
Version 9.0	
After you generate fan-in connections in the Chip Planner, the print preview is blank.	
Version 8.1	
The Altera Complete Design Suite version 8.1 cannot be installed from the default DVD mount point on Red Hat Linux 5.0 32-bit and 64-bit machines.	To install the Altera Complete Design Suite version 8.1 on Linux 5.0: 1. Insert the DVD disc. 2. `Run mount -o ro,nosuid,nodev,uid=0 /dev/`*<cd_device_node>* `/`*<mount_directory>* If you are using CentOS 5, *<cd_device_node>* is **hdc**. 4. Run `/`*<mount_directory>*`/install`.
On Linux, the MegaWizards for ALTFP_INV, ALTFP_INV_SQRT, ALTFP_EXP, and ALTFP_LOG may exit unexpectedly if you don't wait for the resource estimate display to finish updating. For wide data, this update could take several minutes. If you click **Finish** before the resource display is updated, the wizard results are still valid, but the MegaWizard may exit unexpectedly after it completes.	It is safe to ignore this unexpected exit.
Under Linux Red Hat Enterprise version 5 64-bit, opening the Text Editor during a compilation may occasionally cause the Quartus II software to crash.	Wait until the compilation completes before opening the Text Editor.
Version 6.1	
Under some circumstances, your web browser software may fail to launch correctly from the IP MegaStore MegaWizard Plug-In Manager. The web browser defined in the MegaWizard Plug-In Manager for the IP MegaStore inherits the environment settings from the Quartus II software. Specifically, the `LD_LIBRARY_PATH` environment variable may contain entries that conflict with web browsers such as FireFox, preventing them from starting correctly.	Edit the script that launches the web browser to make sure the Quartus II directories are the last entries in the `LD_LIBRARY_PATH` variable.
Version 6.0	
While any shortcut menu is open from an undocked dockable window, if you right-click the title bar, then all activity in the title bar (left-click and drag, shortcut menu, '**X**' close button) stops working.	Display a shortcut menu again and perform any action except right-clicking in the title bar to restore normal operation.

Device Family Issues

Arria II GX

Issue	Workaround
Version 9.0	
Arria II GX transceiver channel reconfiguration support is incomplete in the Quartus II software version 9.0. The reconfiguration Memory Initialization File (**.mif**) required for channel reconfiguration is not generated by the Assembler.	Manually change the device to a Stratix IV EP4SGX230ES device on the **Device** page in the Quartus II software, and compile the design to generate a Stratix IV MIF. This MIF can be used in designs targeting Arria II GX devices, because the subset of features supported by Arria II GX devices are equivalent to those in Stratix IV devices. The `altgx_reconfig` 'error' port is asserted due to this difference, but this error can be ignored.

Cyclone III

Issue	Workaround
Version 9.0 SP1	
In the Quartus II software version 8.0 and later, for designs targeting Cyclone III devices, the Fitter may introduce incorrect logic when you select **Extra Effort** in the **PowerPlay power optimization** option in the **Analysis & Synthesis Settings** page. Designs with M9K memory blocks that use both the clock enable and rden (read enable) signals may be affected.	Select **Normal compilation** for the **PowerPlay power optimization** option. Alternatively, disable Fitter power optimizations on memory blocks only by setting **Optimize Power during Fitting** to **Normal Compilation** on your memory blocks using the Assignment Editor.
Version 8.0	
If you use DDR or DDR2-SDRAM memory interfaces in designs targeting Cyclone III devices, you may receive the following warning from the TimeQuest Timing Analyzer: `Critical Warning: The register <name> fed by pin <DQ or CK0 pin> must be placed in adjacent LAB <name of adjacent LAB> instead of <name of current FF location> to the result.`	If the adjacent LAB is already used by DDIO input registers for other pins, you may receive this warning because no more than two global clocks (inverted clocks are counted separate from non-inverted clocks) may feed a LAB. To fix the warning, you need to move the CK0/CK0# pins to a location with a free adjacent LAB. A possible solution is to swap CK0/CK0# with CK1/CK1# or CK2/CK2#.

When you receive one of the following messages, there is a timing violation issue that needs to be fixed:
`Critical Warning: The register <name> fed by pin <DQ or CK0 pin> must be placed in adjacent LAB <name of adjacent LAB> instead of <name of current FF location> to the result`
`Critical Warning: Fitter could not properly route signals from DQ I/Os to DQ capture registers because the DQ capture registers are not placed next to their corresponding DQ I/Os`
`Info: DQ capture register <name> at <location> is not assigned to the adjacent LAB of the corresponding DQ I/O <name> at <location>`
	Fix the problem to avoid violating assumptions made with the macro timing analysis used for Cyclone III devices. A possible solution is to swap CK0/CK0# with CK1/CK1# or CK2/CK2#.

Stratix

Issue	Workaround
Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.	

Stratix GX

Issue	Workaround
Version 6.0	
Timing simulation performed in the Quartus II software on designs that use the altgxb megafunction in Stratix GX devices is not accurate on the `rx_clkout` and `rx_out` outputs. The simulation is functionally correct, but the relative timing delays between the signals are not accurate.	Perform your timing simulation in another tool such as ModelSim.

Stratix II GX

Issue	Workaround
Version 8.1	
Versions of the Quartus II software earlier than 8.1 allowed illegal GXB configurations with very high PLL input clock frequency and very lower GXB datarate. Compiling these configurations in the Quartus II software version 8.1 produces an error.	For the Quartus II software version 8.1, re-generate the design with the MegaWizard, and change to the frequency and datarate to adhere to the new limits, as necessary.
Version 7.2	
The VCS flag `-ntb_opts +check` can produce the following error when running Synopsys VCS simulation using **stratixiigx_hssi_atoms.v** (alt2gxb simulation library): Error: Illegal array access. This out-of-bound/illegal array access at time 0 happens at unused channels/blocks where default parameter values and initial values of ports are not consistent.	Remove the `+check+` option when compiling **stratixiigx_hssi_atoms.v**. The check is to report specifically out-of-bound or illegal array access (no other type of checking).
Stratix II GX post-fit compiler databases created in the Quartus II software version 7.1 are not backwards compatible with the Quartus II software version 7.2.	Rerun the Fitter after importing Stratix II GX projects compiled in the Quartus II software version 7.1.
Version 6.0	
The latency of alt2gxb megafunction simulations on Stratix II GX is not accurate in comparison to the device. This is due to approximation used in the Quartus II simulation in modeling the analog portion of the hardware. The latency on the digital portion is within the range of a few clock cycles of the device. The latency is an exact match with the hardware when input vectors are carefully made and do not contain any race conditions.	The Stratix II GX Handbook has specified latency range information. The latency information from Quartus II simulations is a good approximation.

Stratix III

Issue	Workaround
Version 8.0	
You may see an Internal Error during timing analysis on a design targeting a Stratix III device to an I/O with a current strength setting of **Minimum Current** or **Maximum Current**.	Replace the current strength setting on the I/O with a correct current strength setting (for example, 12mA), instead of a maximum or minimum.
Version 7.1	
If a design that targets Stratix III devices uses LVDS RX in an I/O row, you cannot use half-rate DDR on the TX pins of the same I/O row. As a result, you cannot use DQ pins of a DDR memory interface together with LVDS RX in any Horizontal I/O row.	

Stratix IV

Issue	Workaround
Version 9.0 SP1	
When you use RX PMA-direct on Stratix IV devices, the timing model in the Quartus II software is incorrect. As a result, the placement algorithm may put a register too close or too far away from the high speed interface. It appears to meet timing in the Quartus II software, but when it runs on silicon, this inaccurate register placement causes timing violations. This issue does not show up in PCS mode because the phase comp FIFO in the PCS resolves this timing issue.	
Version 9.0	
Transceiver designs using the Auxiliary Transmit (ATX) PLL might produce the following error: `Error: ATX Atom "atx_pll" at location "HSSIPLL_X0_Y25_N135" requires a calibration block at location "CALIBRATIONBLOCK_X0_Y2_N135"`	If no existing placed calibration blocks from another transceiver are placed in the corner driving the specified ATX, then one must be implicitly created with a dummy transceiver. Do this by moving or making existing transceiver channel pin assignments in the Pin Planner so that the pins are placed into transceiver blocks 0 or 1 on the same edge of the device as the ATX. You can also create a new transceiver instance of any type and assign one or more pins to the transceiver block 0 or 1 on the same edge of the device as the ATX location.
When you instantiate an altgx megafunction in a design that targets a Stratix IV device and uses Basic (PMA Direct) protocol, ignore the **Logical address of the PLL** on the **Reconfig** page.	

Issue	Workaround
A GPLL is needed to support PMA-direct channels running at higher data rates. Most of the time, the Quartus II Fitter places the GPLL on the same side as the HSSI channel, as expected. However, sometimes the GPLL and the HSSI channel are placed on different sides. As a result, if the channels and the GPLL are placed on different sides of the device, the phase-shifts suggested in the *Stratix IV Handbook* no longer apply, and the design might fail timing.	Make a location assignment to the GPLL to ensure that it is on the same side as the HSSI channel.
In the Quartus II software version 9.0, the alt_oct megafunction works in designs that target the Stratix III device family but failed to begin calibration for the Stratix IV device family.	
Version 8.1	
Starting in the Quartus II software version 8.1, an altgx megafunction in a design that targets Stratix IV devices generates **reconfig_togxb[3:0]** input bus. `Rx_analogreset` is ignored and `rx_pll` may not work properly in Quartus II simulation if these ports are not connected appropriately.	You must connect `reconfig_togxb` with reconfiguration controller because of silicon requirements. For functional simulation or module level simulation, you can connect **reconfig_togxb[3:0]** = **4'b0010** if you do not have a reconfiguration controller in the same scope to connect.
Although the ALTGX MegaWizard allows disabling the **Insertion of deletion of consecutive characters or order sets** option under **Rate Match FIFO** on the **Rate match/Byte** order page, this option should not be disabled.	You must turn on the **Enable insertion or deletion of consecutive characters or ordered sets** option if the ALTGX configuration meets all of the following requirements: • Basic protocol • Double serializer block width • Rate Math FIFO enabled
When you choose a base datarate of 6500 Mbps or more and the effective datarate is 1/2 or 1/4 of the base datarate, only an input clock frequency that is 1/20 the base datarate should be allowed. However, the MegaWizard and Compiler currently allow multiple input clock frequencies.	When you choose a base datarate of 6500 Mbps or more, do not choose an effective datarate that is different from the base datarate.

Issue	Workaround

When you lock a PCS transceiver channel, which is not PMA only, to a central channel (5 or 6) two things might occur:
An internal error:
Internal Error: Sub-system: FHSSI, File: /quartus/fitter/fhssi/fhssi_placer.cpp, Line: 2805
golden_bin == channel_bin
Or a no-fit error:
`Error: Can't place GXB Central Control Unit atom "top_alt4gxb_0es9:top_alt4gxb_0es9_component|cent_unit0" File: D:/designs/tgx/top.v Line: 633`
`Error: Atom "top_alt4gxb_0es9:top_alt4gxb_0es9_component|cent_unit0" of type "GXB Central control unit" cannot be placed at location CMU_X0_Y10_N139 that is in a different transceiver block location than the following atom(s) File: D:/designs/tgx/top.v Line: 633.`
	Remove the location constraint on the pin and/or related atoms or lock the pin down to a regular transceiver channel (1 through 4).

Version 8.0	
Disabling the output termination assignment on a Stratix IV transmitter transceiver pin (Example: `set_instance_assignment -name output_termination OFF -to tx_dataout`) without a valid transceiver I/O standard assignment on the pin will result in the following error: `"Error: One or more pins are missing I/O standard assignments"`	Make a valid HSSI transceiver I/O standard assignment on the pin or enable the `output_termination` setting.
PCIE Gen 2 x8 will have 8 rateswitch control ports (if 8 channels are used) and only `rateswitch[0]` will control the operation. `rateswitch[7:1]` does not have any affect. The same applies to PCIE Gen2 x4 mode (`rateswitch[3:1]` has no affect).	

Stratix IV GX

Issue	Workaround
Version 9.0	

A design implementing HSSI transceivers might not fit with the following error(s):
`Error: Can't place GXB Central Control Unit atom "cent_unit_instance"`
`Error: Atom "cent_unit_instance" of type "GXB Central control unit" cannot be placed at location CMU_X119_Y41_N139 that is in a different transceiver block location than the following atom(s)`
`Info: Atom "refl_clk" of type "I/O pad" is at location IOPAD_X0_Y10_N145`
`Info: Atom "refl_clk(n)" of type "I/O pad" is at location IOPAD_X0_Y10_N147`
`Info: Atom "refl_clk~input" of type "I/O input buffer" is at location IOIBUF_X0_Y10_N146`
	Make the location assignment to pins of transceivers that are clocked by the same reference clock, so that the pins are along the same edge of the device.

Issue	Workaround
Transceiver designs with multiple refclk pins driving multiple transceivers, or with multiple core PLLs driving multiple transceivers, might not fit. Multiple errors such as the following might be given: `Error: Can't place GXB Central Control Unit atom "hsi_rxtx:\g_csg:3:i_csg|hsi_rxtx_alt4gxb_dtu8:hsi_rxtx_alt4gxb_dtu8_component|cent_unit0" File: D:/spr/298480/hsi_rxtx.vhd` `Error: Atom "hsi_rxtx:\g_csg:3:i_csg|hsi_rxtx_alt4gxb_dtu8:hsi_rxtx_alt4gxb_dtu8_component|cent_unit0" of type "GXB Central control unit" cannot be placed at location CMU_X119_Y10_N139 that is in a different transceiver block location than the following atom(s) File: D:/spr/298480/hsi_rxtx.vhd Line: 1508` `Info: Atom "refl_clk" of type "I/O pad" is at location IOPAD_X0_Y10_N145` `Info: Atom "refl_clk(n)" of type "I/O pad" is at location IOPAD_X0_Y10_N147` `Info: Atom "refl_clk~input" of type "I/O input buffer" is at location IOIBUF_X0_Y10_N146`	Make the location assignment to groups of transceiver pins that are clocked by the same refclk or core PLL, so that the pins are along the same edge of the device.

A transceiver design that has dynamic reconfiguration and that targets a Stratix IV GX device may incur the following Internal Error:
`Internal Error: Sub-system: FHSSI, File: /quartus/fitter/fhssi/fhssi_dprio.cpp, Line: 1222`
`m_tx_pma_inclk_regs[i] != 0`
	If you receive this error, you can take one of the following actions:
	■ Regenerate your altgx_reconfig megafunctions in the Quartus II software version 9.0.
	■ Make sure that all input ports of your altgx_reconfig megafunction instances are connected to valid input sources that are not GND or VCC.
	■ Insert LCELL buffers before the `reconfig_mode_sel[2..0]` input ports of your altgx_reconfig megafunction instances.
	■ If your design uses multiple altgx_reconfig megafunction instances, combine them into one instance.

Stratix II GX & Stratix IV

Issue	Workaround
Version 8.0	
When the live I/O check feature of the Pin Planner is turned on and transceiver pins are present in the design, errors similar to the following occur even though the design will pass I/O assignment analysis: `Pin <name> does not support I/O standard <default I/O standard> for <name>`	Manually assign the proper transceiver I/O standard to the pin.

Cyclone, Stratix & Stratix GX

Issue	Workaround
Version 6.0	
The method used to report power for clock networks is different between the Quartus II PowerPlay Power Analyzer and the PowerPlay Early Power Estimator (EPE). The Quartus II PowerPlay analyzer reports the power for the resource (pin or PLL) that drives the network, while the EPE reports the power in the Clock Network section of the spreadsheet.	No action is necessary.

Cyclone III & Stratix III

Issue	Workaround
Version 7.1	
Location and other assignments made to the altpll megafunction name and intended only for the PLL WYSIWYG are also applied to logic cells created by the altpll megafunction. As a result, you may see errors indicating PLL assignments do not apply to logic cell nodes.	Make assignments intended only for the PLL on the PLL WYSIWYG name only and not on the higher-level altpll hierarchy name.

Cyclone III, Stratix III & Stratix IV

Issue	Workaround
Version 8.1	
In the Quartus II software version 8.1, connecting the **stratixiii_crcblock atom** to the dedicated CRCERROR pin in a design causes the pin to be connected using Single Event Upset (SEU)-vulnerable core logic instead of the dedicated route unless the **Enable error detection CRC** option is turned on in the **Device and Pin Options** dialog box.	When instantiating the **stratixiii_crcblock** or **cycloneiii_crcblock** atom, turn on the **Enable error detection CRC** option.

Issue	Workaround
Version 8.0 SP1	
In the Quartus II software version 8.0, incorrect behavior results in designs targeting Cyclone III, Stratix III, or Stratix IV devices when the register has an inverted `sload` signal and the `sdata=GND`, and register is packed into either the output register or input register, then the inversion is lost. This behavior is seen as incorrect because the register clears at the wrong times.	This issue is fixed in the Quartus II software version 8.0 SP1.

Stratix & Stratix GX

Issue	Workaround
Version 6.0	
The Quartus II PowerPlay Power Analyzer reports PLL, XGMII state machine, GXB transceiver, and I/O pin power as contributors to the power reported for High Speed Transceiver blocks. However, the PowerPlay Early Power Estimator (EPE) spreadsheet reports this power in a “High Speed Transceiver Blocks” section as well as an entry in the “Clock Networks” section. Similarly, the PLL, SERDES blocks, and I/O pins of an LVDS block are reported in the PowerPlay Power Analyzer, and as entries in the Clock Networks and HSDI sections of the EPE spreadsheet.	

Stratix II & Stratix II GX

Issue	Workaround
Version 8.0 SP1	
In Quartus II software versions 8.0 and earlier, the altlvds_tx simulation model for EDA simulation shows that the `tx_outclock` signal is edge aligned with the `tx_out` signal when `OUTCLOCK_ALIGNMENT` is **180_DEGREES** and `USE_EXTERNAL_PLL` is **ON**.	Simulate the design in the Quartus II software version 8.0 SP1.

Stratix III & Stratix IV

Issue	Workaround
Version 9.0	
The Serial Flash Loader IP does not function for Stratix III or Stratix IV devices.	

Issue	Workaround
The Quartus II software version 8.1 and version 9.0 incorrectly disable the Parallel OCT on the negative pin of input pairs assigned as Differential SSTL or HSTL I/O standard with Parallel OCT enabled.	To correct this issue, download and install patch 0.55 for Quartus II software version 8.1 and patch 0.03 for Quartus II software version 9.0 from the following locations: ■ Patch for Quartus II software version 8.1: ■ Quartus II 8.1 Patch 0.55 for PC ■ Quartus II 8.1 Patch 0.55 for PC readme.txt ■ Quartus II 8.1 Patch 0.55 for Linux ■ Quartus II 8.1 Patch 0.55 for Linux readme.txt ■ Patch for Quartus II software version 9.0: ■ Quartus II 9.0 Patch 0.03 for PC ■ Quartus II 9.0 Patch 0.03 for PC readme.txt ■ Quartus II 9.0 Patch 0.03 for Linux ■ Quartus II 9.0 Patch 0.03 for Linux readme.txt For further assistance, contact Altera Technical Support by creating a Service Request at **www.altera.com/mysupport** and provide them the reference number **rd03112009_85**.
Version 8.1	
If you instantiated the altlvds_rx megafunction in the Quartus II software versions earlier than 8.1, you receive this error in the Quartus II software version 8.1: `Error: LVDS_RX "rx[0]" has parameter reset_fifo_at_first_lock with illegal value true -- only value false is legal`	Generate the megafunction in the Quartus II software version 8.1.

Arria GX and Stratix IV GX

Issue	Workaround
Version 8.1	
The transmitter analog setting **VCCH** can be set to **Auto** and is automatically promoted to 2.5 or 3.0 volts by the Fitter. An error occurs if the promoted voltage does not match the user-assigned I/O standard on the associated transmitter pin. If it does not match, an error similar to this error occurs: `Error: I/O standard "1.5-V PCML" on I/O pin "tx_dataout[0]" is incompatible the GXB channel's VCCH voltage setting "1.4V"`	Remove the I/O standard setting on the transmitter pin, match the I/O standard on the transmitter pin to the promoted V_{CCH} voltage, or set the V_{CCH} voltage to match the pin's I/O standard.

Arria II GX and Stratix IV

Issue	Workaround
Version 9.0	
For altgx instantiations that have enabled 8b10b encoding, the reported values in the following Compilation Fitter Reports are incorrect, because they do not account for the data width change due to 8b10b encoding. ■ **Core Clock Frequency** in the GXB Receiver Channel Report ■ **Core Clock Frequency** in the GXB Transmitter Channel Report	Multiply the reported values in these fields by 8/10 to account for the data width change due to 8b10b encoding and recover the correct values.
If your transceiver design targeting a Stratix IV or Arria II GX device uses multiple ALTGX_RECONFIG controllers, and any one of these controllers feeds any other controller directly or indirectly (through other logic in the design), you may run into Fitter internal errors or get incorrect post-layout simulation results.	Combine these controllers into a single controller.

HardCopy

Issue	Workaround
Version 9.0 SP1	
If a clock/clear signal drives RAM slices that are placed in a MLAB using a global/regional/periphery clock, and also drives other logic using normal routing, then the global signal usage may not be properly back-annotated to the HardCopy III/HardCopy IV revision. This action can cause problems such as not being able to reproduce the same register packing as the companion Stratix III/Stratix IV revision (if the Fitter packs registers into these RAM slices), and failure to compare revisions with the **Compare Revision** dialog box.	Either do not allow the Fitter to place these RAM slices into MLABs, or ensure that such signals do not use normal routing to drive other logic.
In the Quartus II software version 9.0 SP1, compilation for HardCopy III WB devices and HardCopy IV GX devices is not supported, but these devices are still visible in the Quartus II GUI.	
Version 8.0	
Behavior of region constraints on HardCopy II is changed in the Quartus II software version 8.0 such that all HCell-based logic must be placed within the region boundaries. In Quartus II software versions 7.2 SP3 and earlier, this restriction was not necessary, and there was a 20 HCell tolerance at region boundaries. This new behavior allows you to enable more advanced incremental compilation flows.	The change in behavior can cause no-fits because the available area for a region constraint is now smaller than in earlier releases. You may need to increase region sizes in order to achieve a fit.
Version 7.2	

Issue	Workaround
When compiling a HardCopy II design and using the HardCopy II Advisor to compare timing against the Stratix II FPGA flow, the timing for the I/Os may be different. This difference is because the FPGA compilation used Advanced I/O Timing, which is unsupported for HardCopy II devices, to get I/O delays.	When compiling the FPGA, disable Advanced I/O Timing by setting the Quartus II Settings File (**.qsf**) assignment `ENABLE_ADVANCED_IO_TIMING` to `OFF` or turn off **Enable Advanced I/O Timing** in the **Timing Quest Timing Analyzer** page in the **Settings** dialog box.
Version 6.0	
Under certain circumstances, you may receive the following error message when migrating your Stratix II design that contains RAM blocks to HardCopy II: `"Error: Source file <file> in directory <dir> was compiled at <time> and saved at <time>. The problem reported for the file is: Only in HardCopy II (<design>)."`	Turn off the **Auto RAM Block Balancing** option for your Stratix II design and recompile the design. Then proceed with the migration process.

EPC2 Configuration Devices

Issue	Workaround
Version 6.0	
When using the EPC2 configuration device to configure an Altera FPGA using a compressed configuration bit stream, you may encounter a configuration failure due to the CONF_DONE error checking feature. The failure mode occurs when the FPGA releases the CONF_DONE signal outside the acceptable time window. The reason this may occur is because the compression ratio varies depending on the design file. Since the configuration file size varies due to compression there may be insufficient padding at the end of the configuration file. This issue can result in a configuration failure, as indicated by the nSTATUS pin transitioning low near the end of configuration. The error occurs because the CONF_DONE signal is released by the FPGA before the EPC2 device expects it to be released.	For assistance implementing the workaround, contact Altera Technical Support at **www.altera.com/mysupport** and provide the reference number **rd01232008_817**.

SOPC Builder Issues

Issue	Workaround
Version 9.0	
The TimeQuest Timing Analyzer may report recovery path failures from the SOPC Builder–generated reset synchronizers to the clock crossing bridge's internal dcfifo asynchronous clear signal.	These failing recovery paths may be safely declared as false paths in your design.
hw.tcl components cannot be instantiated or edited if any non-string parameters have allowed ranges with display labels. Example range with labels: `set_parameter_property RESPONSE_PORT ALLOWED_RANGES { "0:Memory-Mapped" "1:Streaming" "2:Disabled" }`	Use values without labels in the allowed ranges, or use string parameters. Example range without labels: `set_parameter_property RESPONSE_PORT ALLOWED_RANGES { 0 1 2 }`

Adding labels to the ALLOWED_RANGES property for a non-String parameter results in a component that you cannot instantiate or edit. For example, the following Tcl code does not compile in the Quartus II software version 9.0:
`add_parameter RESPONSE_PORT INTEGER 0`
`set_parameter_property RESPONSE_PORT ALLOWED_RANGES { "0:Memory-Mapped" "1:Streaming" "2:Disabled" }`
	Do not use labels in the ranges or use string parameters. For example, the following Tcl compiles in 9.0:
	set_parameter_property RESPONSE_PORT ALLOWED_RANGES { 0 1 2 }

The On-Chip FIFO Memory component, when used in dual-clock mode, does not properly synchronize some control signals between the two clock domains. This issue can cause timing failures in designs that use the component.	
The *Component Interface Tcl Reference* chapter in volume 4 of the *Quartus II Handbook*, incorrectly lists `TERMINATION_WIDE` as a parameter to the `get_port_properties` command. The correct parameter is `TERMINATION_VALUE`.	
Version 8.1	
For parameters of type `std_logic_vector`, component authors cannot set the vector's width from within Component Editor.	After saving the **_hw.tcl** file in Component Editor, modify the **_hw.tcl** file to add the parameter's range. The width of the `std_logic_vector` parameter is derived from the range. For example, a range of `0..511` would imply 1 9-bit vector.
The `--jdi` option scans the JTAG chain, gets the first device it finds from the JTAG chain, and applies the JDI information to that device node blindly.	If there is more than one device in the chain, please load JDI information using the new **device_load_jdi** command as part of the device service, inside System Console. With that command, specify the virtual file system path to the device node of interest, so that there is no ambiguity.

Issue	Workaround

In the Quartus II software versions 7.1 SP1 and later, you may encounter the following error if you have McAfee VirusScan 8.0.0 Enterprise Edition installed during system generation in SOPC Builder or while doing a build in the Nios II IDE.
`4 [main] ? (3920) C:\altera\80\quartus\bin\cygwin\bin\sh.exe: *** fatal error - couldn't allocate heap, Win32 error 487, base 0x6D0000, top 0x6F0000, reserve_size 126976, allocsize 131072, page_const 4096`
`3 [main] sh 420 fork: child -1 - died waiting for longjmp before initialization, retry 0, exit code 0x100, errno 11`
	Either temporary disable McAfee VirusScan 8.0.0 or upgrade to VirusScan 8.5.0i.

In previous versions of SOPC Builder, if your **_hw.tcl** file didn't match the HDL file, the **_hw.tcl** file was considered the correct file. In the Quartus II software version 8.1, the HDL file is considered the correct file. If correct functioning of your component relies on the **_hw.tcl** file description overriding the HDL description, your component may not operate correctly.	Ensure that the description of your component that you provide in your **_hw.tcl** file matches the HDL.
Incorrect clock interface wiring in generated HDL can occur when Tcl-based components containing clock sources are used. The problem is caused by an incorrect setting in the component hardware Tcl file, for example: `set_interface_property clock_source ptfSchematicName` Component Editor makes this incorrect assignment when clock source interfaces are created.	To resolve the problem, change the **ptfSchematicName** value to a system-unique string value, rather than an empty string. A sensible value to use is the name of the clock source interface, but this does not work if multiple instances of the clock-sourcing component are used. To support multiple instances, the component can provide a string parameter, which you must assign with a system-unique value. The clock-sourcing component can make the **ptfSchematicName** assignment from this string parameter in an elaboration callback.
Version 8.0	

Issue	Workaround
The system interconnect fabric that is automatically created when you generate your system in SOPC Builder does not correctly resolve the bytes that are not selected by the byteenable lines on a 64-bit write to a 32-bit Avalon-MM slave interface with no byteenable capability. If a master module sends a 64-bit write request to a system component 32-bit Avalon-MM slave interface, the write arrives at the slave port as two separate 32-bit writes to consecutive addresses. If the byteenable lines indicate a single 32-bit write to the destination address, because the byte enables are not asserted for the second half of the 64 bits, the write nevertheless occurs at both addresses. Therefore, if the byteenable lines for the second half of the 64-bit write are not asserted, the address following the destination address is written erroneously.	Perform the following workaround for each 32-bit, byteenable-free slave port in your SOPC Builder system component: 1. In SOPC Builder, on the **System Contents** tab, add an Avalon-MM Pipeline Bridge component. 2. In the Avalon-MM Pipeline Bridge editor, under **Pipeline** options, configure the pipeline bridge with all three pipeline options turned off. 3. Under **Data** options, set **Data width** to 32 bits. 4. Under **Burst** options, turn on **Allow bursts** and set the **Maximum burst size** to **2**. 5. Connect the Avalon Memory-Mapped Master Port of the pipeline bridge to the slave port in your SOPC Builder system component. 6. Connect the Avalon Memory-Mapped Slave Port of the pipeline bridge to the master module that would otherwise be connected directly to the slave module.
A component originally provided and created with SOPC Builder component version 7.2 with multiple clock ports generates an error in the Quartus II software version 8.0.	Edit the Tcl Script File (**.tcl**) associated with the component to remove any derived clocks. This clocking scheme is not supported for the component.
The System Console hangs with the message `NIOS2OCI::internal_unlock(): Assertion `m_locked' failed.` when accessing a service provided by a Nios II processor and services provided by other modules simultaneously.	Open as many System Consoles as are required before issuing any commands to any of them.
When masters execute write transactions to narrower-data width slaves, unintended write transactions can occur. The problem can occur only for dynamically-aligned slaves that do not have byteenable ports.	When possible, dynamically-aligned slaves should be provided with byteenable ports. In cases where the slave component cannot be modified, a simple workaround for this problem is to insert an Avalon-MM pipeline bridge in between the master and slave. (If this bridge is configured with all three of its pipeline options turned off, the component consists only of wires, and thus consumes no logic resources.)
Tooltip information entered into Component Editor is not saved in the component's Tcl Script File (**.tcl**).	The tooltip can be added to the Tcl Script File manually as the last argument to the **add_parameter** command.
If VHDL components have a generic of type **'std_logic_vector'**, the width of the vector cannot be greater than 32 bits.	Use generics of type **integer**, or that are less than 32 bits wide.
On systems where adapters are inserted in front of the widest Avalon-MM slave in the system, generation may fail with the following message: `Base address for module_name must be a multiple of its span`	Manually readdress the slaves according to the span provided in the error message.

Issue	Workaround
On Windows Vista-64, when using the 64-bit version of the Quartus II software, SOPC Builder occasionally hangs while generating the system, or while upgrading SOPC Builder system version 6.2 or earlier.	Use 32-bit version of the Quartus II software instead of the 64-bit version.
The Nios II processor is configurable and may or may not include an MMU, MPU, and extra exception (EE) handling. However, the System Console always presents all registers from these modules as a response to **processor_get_register_names**, even when these registers don't exist. Reading MMU, MPU, and extra exception handling registers when they don't exist returns the value of other registers.	Don't read registers in the MMU, MPU, or EE modules when the Nios II processor does not include these options.
Version 7.2 SP1	
Access to bursting components, such as DDR SDRAM, may fail in SOPC Builder.	The cause for some bursting failures is related to the different bursting capabilities of Avalon-MM master and slave ports. DDR SDRAM supports burst wrapping whereas other components do not. To resolve this issue, ensure that burst boundaries are not crossed during burst transactions.
Version 7.2	
In a Nios II system, if you turn on **Enable bursts** for the **Data master** settings in the Nios II processor, data master burst reads of size > 1 from unassigned locations result in system lockup.	Avoid making data master reads from unassigned locations.
When a latent-aware Avalon master does a read access to a nonexistent location, the Avalon bus fabric returns a dummy response so that the reading master does not stall. However, only a single response (`readdatavalid` pulse) is returned. If a burst read is done to a nonexistent location, the bursting master receives only the single response, and stalls while awaiting the remaining `readdatavalid` pulses.	
SOPC Builder generation may fail with Java errors when the system is generated from the command line using a Tcl script. These errors occur if no Xserver is running on your machine.	Set up an Xserver on your machine and regenerate the SOPC Builder system.
The SOPC Builder may generate errors regarding address span overlap when generating systems with bursting masters and wide data path widths of 32 bits or more.	Move the native addressing components farther apart so that base addresses won't overlap even if the span grows by a factor of 2 (or 4 if the data width is 128 bits).
Version 7.1	
Custom components created in versions of SOPC Builder earlier than 7.1 that have data widths that are not multiples of two and greater than 8 bits will not upgrade properly.	Import your custom logic into Component Editor and specify a data width that is at least eight bits wide and a multiple of two (8, 16, 32, 64, etc...) If you increase the width of your component to comply with these limits, the Quartus II software automatically removes any unused bits during synthesis.

Issue	Workaround
An Avalon-MM master connected through an Avalon-MM pipeline bridge or Avalon-MM clock crossing bridge to Avalon-MM slaves that use native addressing will fail if the bridge is wider than the master.	Do not connect a narrow Avalon-MM master to a wider Avalon-MM bridge if that master accesses an Avalon-MM slave that uses native addressing through the bridge.
The Component Editor in SOPC Builder does not support Verilog HDL design files (**.v**) that have multiple modules or VHDL design files (**.vhd**) with multiple entities.	Use only one module for each Verilog HDL design file and one entity for each VHDL design file.
If a module dependency loop is reported between the DMA controller and pipeline bridge, the resulting system may still be functional.	The system can be generated by holding down Ctrl and clicking the **Generate** button.

EDA Integration Issues

Issue	Workaround
Version 9.0	
Mentor Graphics ModelSim 6.4a has a known issue in which a GUI query for design information may appear to slow during the loading of a design, after compilation. This behavior is more noticeable for large scale designs, especially those with transceivers. However, the GUI is not actually frozen, and the design is loaded with a longer than usual time.	This issue is fixed in Mentor Graphics ModelSim versions 6.4b and later.

VHDL simulators such as Mentor Graphics ModelSim and Cadence NCSim software produce warnings such as the following when simulating designs that include altgx MegaWizard-generated designs targeting Stratix IV and Arria II GX devices:
`Time: 114168 ps Iteration: 52 Instance: /gx_reconfig/b2v_u_altgxb/b2v_inst/gxb_sts12_alt4gxb_pc3b_component/transmit_pcs0/digi_tx_1/tx_ctrl_1/ph_fifo_tx_1`
`# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).`
	To turn off the warnings from the ModelSim software:
	1) In the **$modelsim_instal_dir/modelsim.ini**, type the following:
	`; Turn off warnings from the std_logic_arith, std_logic_unsigned`
	`; and std_logic_signed packages.`
	`StdArithNoWarnings = 1`
	`; Turn off warnings from the IEEE numeric_std and numeric_bit packages.`
	`NumericStdNoWarnings = 1`
	Or, in the ModelSim software, run **script**:, and then add this line after loading:
	`set StdArithNoWarnings 1`
	2) In the Cadence NCSim (NC-VHDL)software:
	a) At the NCSIM command prompt, type:
	ncsim> `set pack_assert_off {std_logic_arith}`
	b) NCSIM run **script:**
	c) Create a text file, for example, **run.do**, with the following content:
	set pack_assert_off {std_logic_arith}
	run

If you are using the Cadence NCSim (NC-VHDL) software for reconfiguration with the altgx_reconfig megafunction, the **ncelab** command requires a `-relax` option.	Use the `-relax` option.
Version 8.1	
ModelSim version 6.3g has optimization turned on by default. Optimization can generate incorrect simulation results, especially when there is a race condition or there are unconnected input ports in Verilog designs.	Turn off optimization in one of the following ways: ■ Comment out the following line in your **modelsim.ini** file: `;VoptFlow = 1` ■ Specify `-novopt` with the **vsim** command.
Version 8.0	

Issue	Workaround
The clock path delays reported by the PrimeTime software may not be accurate for Stratix III family, due to a limitation in min/max clock path modeling. The clock path delays reported by the PrimeTime software may be off by a few hundred picoseconds, compared to those reported by the TimeQuest Timing Analyzer.	
The Quartus II software may show false errors when you exit the Aldec Active-HDL 7.3 GUI containing the waveform window, when the Active-HDL 7.3 GUI was launched via the NativeLink interface.	Set waveform mode to standard waveform in Active-HDL 7.3 GUI by running the command **waveformmode awf**, either from the Active-HDL console window or from within the do file, before initializing simulation. You need to complete this process only once because the waveform mode is stored in the registry.

If you want to upgrade to Mentor Graphics ModelSim 6.3f release, which is more recent than the Altera-supported version of 6.1g, you can expect some speed up in simulation time. However, there are known issues with the 6.3f release.	Possible solutions include the following:
	For designs that are giving incorrect simulation results, turn off the optimizer by commenting out the following line in the **modelsim.ini** file:
	`; VoptFlow = 1`
	If you use altera_mf.vhd and simulate altsyncram model, avoid the known bug in version 6.3f by typing the following:
	`vcom -opt=-clkOpt altera_mf.vhd`
	instead of the normal compilation:
	`vcom altera_mf.vhd`

Version 7.2	
When reporting timing, the Synopsys PrimeTime software issues an error message (UITE-461) that states that **rise_edge** or **fall_edge** cannot be satisfied, and assumes zero source latency for certain derived clocks.	Set variable **timing_edge_specific_source_latency** to **false** in the PrimeTime shell before reporting timing.
Mentor Graphics ModelSim Altera Edition 6.1g and the ModelSim SE 6.1g software may run out of memory with an error on the Windows platform, when compiling or simulating a large post-fit netlist.	Use a 64-bit computer running the Linux operating system to compile and simulate the design. Contact Mentor Graphics for additional support.
Version 6.1	

Issue	Workaround
If there are virtual I/O pin assignments at the time of generating board-level timing files in the STAMP format, and if there is any other tool or format selected in any EDA tool category on the **EDA Tool Settings** page, you may receive an error when you run the EDA Netlist Writer.	If the design has virtual I/O pin assignments, and you want to generate board-level timing files in the STAMP format, then either remove the virtual I/O pin assignments from the Quartus II Settings File (**.qsf**) and recompile the design, or make sure the following is true before running quartus_eda: All tool and format settings in all categories are set to None with the exception of Board-Level timing analysis tool category. STAMP is selected as the EDA format in the **Board-Level Timing Analysis** tool category in the **Board-Leve**l page under **EDA Tool Setting**s. Or, you can run the following command at a system command prompt: `quartus_eda --format=stamp --board_timing` *<project>* `-c` *<revision>*
Version 6.0	
The ModelSim software may fail to simulate a design if **Glitch Filtering** is turned on in the EDA Simulation Settings page and the `+nospecify` option is passed to the ModelSim **vsim** command.	Remove the `+nospecify` option from the ModelSim **vsim** command.
If you add or change a component in a Library Mapping File (**.lmf**), the Quartus II software does not recognize the changes upon the next compilation.	Delete the project database (**db**) directory and recompile.

Memory Interface Issues

Issue	Workaround
Version 9.0 SP1	
During timing analysis, a warning regarding the PLL bandwidth setting may appear when there are cascading PLLs driving the ALTMEMPHY megafunction: `"Critical Warning: ALTMEMPHY PLL, <PLL name>, when fed by another PLL, must have bandwidth mode set to High instead of Auto"`	Set the bandwidth setting to High for the PLL using the ALTPLL megafunction.
DDR3 SDRAM without leveling configurations are supported up to a maximum of 400MHz on Stratix III and Stratix IV devices on -2 and -3 speed grade parts. If you select this configuration for a memory clock frequency greater than 400MHz in the ALTMEMPHY megafunction or DDR3 SDRAM High Performance Controller IP MegaWizard for -2 speed grade devices you are not alerted to the fact that above 400MHz is unsupported, and in addition, you see the following erroneous message: `“Info: Calibrated dynamic read and write deskew enabled for DDR3 SDRAM above 400MHz”` The message is intended for leveling configurations and has no effect outside that configuration. The without levelling configuration is selected by choosing **Discrete Device** as the **Memory Format** in the MegaWizard.	Do not select a memory frequency above 400MHz for DDR3 SDRAM without levelling configurations.
Version 9.0	

Issue	Workaround

There is a possibility that designs with DDR3 ALTMEMPHY megafunctions that target Stratix III or Stratix IV devices can fail setup timing on the **mem_ck/mem_ck_n** generation path. The TimeQuest Timing Analyzer reports a setup failure on a path similar to the following:
From node:
`..._phy_alt_mem_phy_inst|clk|half_rate 1.pll|altpll_component|auto_generated| pll1|clk[0]`
To node:
`..._phy_alt_mem_phy_clk_reset:clk|DDR_ CLK_OUT[0].phase_align_memclk_gen.mem_ clk_opa~DFFPHASETRANSFER0`
Launch clock :
`...altpll_component|auto_generated|pll 1|clk[0] (INVERTED)`
`Latch clock : ...altpll_component|auto_generated|pll 1|clk[3] (INVERTED)`
The path is related to logic used to disable the memory clock. The disable control signal is driven from two sources, one in the controller and one in the PHY. The PHY deasserts the control signal whilst the memory is held in reset and so the PHY source can be ignored.
Please note, memory clock disable in this context refers to **mem_ck/mem_ck_n** and not the separate clock enable signal, mem_cke.
	For the memory controller, there are two scenarios:
	■ Altera's High Performance Controller is being used. In this case, the disable signal is not driven and so the timing failure can be ignored.
	■ A proprietary or third party memory controller is being used. In this case, we advise that the clock disable feature is not used.

Stratix IV external memory interfaces may malfunction in hardware when reading from memory due to hold errors caused by excessively large input delay chain settings on DQ pins.	For further assistance, contact Altera Technical Support by creating a Service Request at **www.altera.com/mysupport** and provide them the reference number **rd03042009_673**.
Designs with ALTMEMPHY IP (But not DDR/2/3 HP Controller IP) and that target Stratix III and Stratix IV devices, when configured with single-ended DQS, may fail with the following fitter error: `Error: Bidirectional I/O "mem_dqs_n[0]" uses parallel termination, but does not have dynamic termination control connected File: design_top.v(hd)` This error occurs because the `mem_dqs_n` (or `mem_dqsn` for non-AFI) bidirectional I/O is present in the top level PHY I/O and is also referenced in the ***<variation>*_pin_assignments.tcl script**, but there are no I/O elements for DQSN present in the IP.	No connections should be made to the PHY's `mem_dqs_n` (`mem_dqsn`) port when it is instanced, and the references to `mem_dqs_n` (`mem_dqsn`) in the ***<variation>*_pin_assignments.tc**l script should be deleted. The design should then compile and fit successfully.

Issue	Workaround
Some DDR3 SDRAM memory presets used by the ALTMEMPHY and DDR3 HP Controller IP have been updated in the Quartus II software version 9.0. If you are migrating existing designs from the Quartus II software version 8.1 to 9.0, you may find that the memory preset parameters in your design were not updated with the 9.0 changes even though you re-generated the core. The presets affected by this change are Micron MT8JTF12864AY-1G1, Micron MT8JTF25664AY-1G0, and Micron MT41J128M8BY-187.	In the ALTMEMPHY MegaWizard GUI, select any different memory preset and then re-select the original preset (remember to re-do any modifications to the preset such as DQ width, CAS latency, and so on). Click **Finish** to re-generate the core.
The ALTMEMPHY megafunction for DDR3 SDRAM on Stratix III and Stratix IV devices in the Quartus II software version 9.0 has the following hardware, compilation, and simulation support. Hardware support: ■ x4 and x8 DDR3 SDRAM in UDIMM, SODIMM and MicroDIMM format ■ x4 and x8 DDR3 SDRAM device support up to and including 80-bit interface widths. DDR3 SDRAM interfaces using components must follow Altera-recommended layout guidelines ■ Single chip select support ■ 300MHz to 533MHz full hardware calibration Simulation support: ■ Skip calibration simulation between 300 and 400MHz for x4 and x8 DDR3 SDRAM (DIMMs) ■ Quick calibration simulation between 300 and 533MHz for x4 and x8 DDR3 SDRAM (DIMMs) ■ Full calibration simulation between 300 and 533MHz for x4 and x8 DDR3 SDRAM (DIMM)	
When generating a DDR3 SDRAM core in x4 mode, the MegaWizard GUI gives the following warning: `Warning: DDR3 SDRAM with "DQ bits per DQS bit" setting of 4 is not currently operational in hardware. You can use it for IO assignment checking and functional simulation in "Skip Calibration" mode.`	This warning can be ignored for IP generated with the Quartus II software version 9.0.
Designs with ALTMEMPHY or DDR/DDR2 HP Controller IP on Stratix III or Stratix IV that target DDR or DDR2 SDRAM memory with the CAS3 setting in half-rate mode and use the AFI option are susceptible to fail in hardware. This is caused by the address/command pipeline depth being set too low for CAS3 operation, and it must be increased by one to avoid potential failures in the postamble protection logic.	For further assistance, contact Altera Technical Support by creating a Service Request at **www.altera.com/mysupport** and provide them the reference number **rd03202009_961**.

Issue	Workaround
If your Stratix IV memory interface design uses DQ data groups that wrap between vertical and horizontal (hybrid) I/O banks, you will receive the following compilation error in the Quartus II software versions 9.0 and earlier: `Error: Cannot place DQ I/O "mem_dq[nn]" to I/O location Pin_Nn since its memory interface I/O group cannot be placed`	For further assistance, contact Altera Technical Support by creating a Service Request at **www.altera.com/mysupport** and provide them the reference number **rd02222009_659.**
In the Quartus II software version 8.1 and earlier, when you turn on **Full Rate with Dynamic Termination** in the ALTMEMPHY MegaWizard for a design with DDR2, the Write DQS strobe edges are missing from the writer transaction that directly follows the previous read. Typically, 6 DQS edges are observed as opposed to the expected 8.	Recompile your design in the Quartus II software version 9.0 with the ALTMEMPHY megafunction.
Version 8.1	
ALTMEMPHY QDRII variations generated in the Quartus II software version 8.0SP1 or earlier using pseudo-x36 mode exits in the TimeQuest Timing Analyzer with an error that includes `Missing Stratix III timing model for derated tSW of HSTL_I HPAD`	Re-generate the ALTMEMPHY variation with the ALTMEMPHY MegaWizard in the Quartus II software version 8.1.
Version 8.0 SP1	
Designs with the QDRII ALTMEMPHY megafunction could fail due to an incorrect `mem_doff_n` operation. Calibration could begin before the required 2048 clock cycles (to allow the DLL on the memory device to lock) following the deassertion of `mem_doff_n`.	The ALTMEMPHY megafunction in the Quartus II software version 8.0 SP1 contains logic to ensure this condition will not occur. Regenerate the QDRII ALTMEMPHY megafunction with the Quartus II software version 8.0 SP1.
Designs with the ALTMEMPHY megafunction generated in the Quartus II software version 8.0 or earlier and that target Stratix III devices for DDR or DDR2 SDRAM interfaces have insufficient SDC timing constraints on the datapath reset logic. This may cause the design to fail power up calibration in some cases.	Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0 SP1 to update the SDC timing constraints.
Designs with the ALTMEMPHY megafunction or the DDR/DDR2 SDRAM High Performance Controller IP created in the Quartus II software version 8.0 that target DDR or DDR2 SDRAM could fail to calibrate correctly in hardware under certain conditions. All variations and device families are potentially affected by this issue.	Regenerate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0SP1.
Version 8.0	

Issue	Workaround
The SDC and Tcl scripts generated in Quartus II software versions 7.2 SP3 and earlier for all ALTMEMPHY-based memory interfaces (including the DDR High Performance Controller, the DDR2 High Performance Controller, and the DDR3 High Performance Controllers for all device families) are incompatible with the Quartus II software version 8.0. Compilation may fail in the Fitter with the error: `Error: can't read "pll_ref_clk": no such variable` and timing analysis will not run. This error occurs because the node types in the timing netlist generated by the TimeQuest Timing Analyzer in the Quartus II software version 8.0 are different from those generated in version 7.2. An SDC update is required to traverse it correctly.	Regenerate the ALTMEMPHY megafunction with the Quartus II software version 8.0.
When you compile an ALTPMEMPHY QDRII/QDRII+ SRAM interface in the Quartus II software version 8.0, you may receive this error: `Error: Bidirectional I/O "mem_dqsn[0]" uses parallel termination but does not have dynamic termination control connected`	Regenerate the ALTMEMPHY megafunction with the Quartus II software version 8.0, or change the bidir pins `mem_dqs`, `mem_dqsn`, and `mem_dq` into input-only pins.
The default t_{DS}, t_{DH}, t_{IS}, and t_{IH} parameters in the ALTMEMPHY and DDR2/DDR3 High Performance Controller MegaWizard Plug-in Manager may be too optimistic, and so the timing analysis is too optimistic. These values need to be adjusted based on the specifications of the memory device and their board slew rates.	Make sure that the memory parameters t_{DS}, t_{DH}, t_{IS}, and t_{IH} entered into the MegaWizard are referenced to VREF instead of to VIH or VIL. Referencing to VREF should include the time for the signal to go from VREF to VIH/VIL. The nominal slew rate for our devices is 1 V/ns for single-ended outputs and 2 V/ns for differential outputs. The computation should be: (differential DQS) $t_{DS} = t_{DSa}$(base)+ VIH(ac)min/DQ_slew_rate (differential DQS) $t_{DH} = t_{DHa}$(base) + VIH(dc)min/DQ_slew_rate (single-ended DQS) $t_{DS} = t_{DS1a}$(base)+ (VIH(ac)min / DQ_slew_rate) + (VIH(dc)min / DQS_slew_rate) (single-ended DQS) $t_{DH} = t_{DH1a}$(base) + (VIH(dc)min / DQ_slew_rate) + (VIH(dc)min / DQS_slew_rate)= $t_{IS} = t_{IS}$(base) + VIH(ac)min/addr_cmd_slew_rate $t_{IH} = t_{IH}$(base) + VIH(dc)min/addr_cmd_slew_rate
The calibration sequencer in the ALTMEMPHY megafunction for QDRII SRAM interfaces has been updated to make the calibration algorithm more robust under certain hardware conditions.	To guarantee reliable calibration, regenerate all QDRII and QDRII+ SRAM ALTMEMPHY variations in the Quartus II software version 8.0.

Issue	Workaround
If you generate a DDR/DDR2/DDR3 HP Controller or ALTMEMPHY with **Enable dynamic parallel on-chip termination (OCT)** turned on, and then re-generate with it turned off, you will have the old OCT assignments still preset.	To avoid this issue, either remove all assignments from your project before running the assignments script from the re-generated project, or use the Pin Planner to apply the assignments in the first instance, and re-generate the assignments. The Pin Planner should then remove the old assignments when you update the IP instance.
If the PLL reference clock IO voltage does not match the IO voltage of your memory interface, you receive "no fit" errors on DDR/DDR2/DDR3 HP Controller or ALTMEMPHY of the form: Error: Can't use clock type External Clock Output at location CLKCTRL_PLLL2E1 for clock control block or source node <snip>altmemddr2_phy_alt_mem_phy_ clk_reset_siii:clk|mem_clk_2x with clock type Dual-Regional Clock -- clock types do not match	To resolve the issue, make sure to set an I/O standard on the PLL input clock that has the same voltage as that for your memory interface.
Cyclone III DDR/DDR2-SDRAM High Performance Controller IP generated prior to the Quartus II software version 8.0 will show the following warning message: `Read and write timing characteristics of memory interface <instance name> are preliminary`	To remove the message, re-generate the memory interface using the IP generated in the Quartus II software version 8.0.
Designs with the ALTMEMPHY megafunction created in the Quartus II software version 7.2 SP3 and earlier that target Stratix III devices for full-rate DDR or DDR2 SDRAM interfaces incorrectly handle incomplete write bursts causing the remaining write operations in the burst not to be masked due to the DM signals not being returned to the high state.	Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0.
The Quartus II software does not automatically place the CK/CK# pins for DDR/DDR2/DDR3 memory interfaces on the same edge as the interface's DQ pins. As a result, you may see the following warning message: `Critical Warning: Pin <CK pin> must be placed on a <edge> I/O to match the path of the read data pins`	Place the specified CK pin on the specified edge of the device.
The ALTMEMPHY megafunction does not guarantee timing closure when address and command signals are on a side that is across from the DQS/DQ pins (for example, DQS/DQ pins are on the top side and address/commands are on the bottom side of the device).	Some of the Stratix IV GX devices do not have user I/Os on the left/right I/O banks as the banks are used for transceivers, forcing the address and command signals to be in the same bank as the DQS/DQ pins limiting the width of your memory interface.
RLDRAM II Controller MegaCore functions that were generated in the Quartus II software versions 7.2 SP3 and earlier are missing timing constraints for the capture data between IOE and the FPGA fabric.	Regenerate the RLDRAM II Controller MegaCore function, and rerun DTW. For detail information, please refer to the *MegaCore IP Library Release Notes and Errata* on the Altera website.

Issue	Workaround
Version 7.2 SP1	
Designs with the ALTMEMPHY megafunction and that target Stratix II devices for 333 MHz DDR2 SDRAM interfaces may not meet setup timing on the postamble paths in a default compilation.	Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 7.2 SP2. Place the registers manually on the resynchronization and postamble paths close to the I/O pins. Postamble setup slacks may be further increased in ~50 ps increments by applying the **DQS Bus to Input Register Delay** logic option in the Assignment Editor to the DQS pin names to increment the slack to the DQS pins in the interface, but with the trade-off cost of decreased postamble enable/disable setup slack. If you use the logic option to increase the delay, make sure your design meets timing on all postamble and postamble enable/disable paths.
The ALTMEMPHY megafunction does not support DDR SDRAM with **CAS Latency** setting **2.0** or **2.5** on the Stratix III device family. The MegaWizard does not enforce this restriction, and selecting this option will create a non-working design.	Use a **CAS Latency** setting of **3.0**.
Version 7.2	
If you have, in the same project, more than one ALTMEMPHY variation generated in different versions of the Quartus II software, you may see a Verilog syntax error reported by synthesis. This error is caused by a common file used by all ALTMEMPHY variations, that has changed from an earlier version of the Quartus II software.	Open all the variations in the ALTMEMPHY MegaWizard in the latest version of the Quartus II software and regenerate them.
The Quartus II software version 7.2 does not support automatic placement of the write data clock output pins when you use the ALTMEMPHY megafunction. For Stratix III DDR/DDR2/DDR3 SDRAM High Performance Controllers, the Quartus II software automatically places the write data clock output pins correctly, but not for the QDRII+/QDRII SRAM ALTMEMPHY interface.	If your design targets Cyclone III or Stratix III devices, fix this issue by regenerating the memory interface IP in the Quartus II software version 8.0. However, if you use Pseudo x 36 mode for QDRII-SRAM or QDRII+-SRAM on Stratix III devices, place the `mem_clk` pin for clocking write data on a DQS pin for QDRII+/QDRII SRAM memory interfaces.

Simulation Model Changes

altera_mf Models

Model	Changes
altlvds	■ Change `rx_dpa_locked` behavior to be asserted according to the new DPA lock circuitry in both internal and external PLL mode. ■ Added support for new DPA switching algorithm in Arria II devices, which is used when parameter `enable_dpa_calibration` is set to ON.
altsyncram	■ Added support to display module and instance name in warnings and errors for Verilog model.

Important: **Altera_mf.v** no longer supports Verilog 1995 standard.

Latest Known Quartus II Software Issues

For more information about known software issues, look for information in the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

Software Issues Resolved

This section list the numbers of the Customer Service Requests that were fixed or otherwise resolved in this version of the Quartus II software.

Customer Service Request Numbers Resolved in this Release			
10657121	10667681	10667950	10669318
10669432	10669530	10669865	10670049
10670776	10672369	10672678	10675281
10675728	10679646	10679651	10680452
10681516	10681806	10682673	10682914
10683496	10684003	10684307	10684800
10685168	10686056	10686150	10686197
10686255	10686606	10686823	10687152
10687808	10687880	10687936	10688063
10688160	10688170	10688219	10688303
10688336	10688657	10688694	10688714
10688721	10688751	10688976	10689225
10689625	10689878	10689929	10690066
10690096	10690660	10690695	10690734
10691077	10691146	10691150	10691361
10691523	10691526	10691614	10691650
10691668	10691800	10692020	10692364
10692921	10693218	10693249	10693614
10693996	10694022	10694185	10694364
10694373	10694469	10694616	10694718
10694723	10694793	10695062	10695102
10695744	10695773	10696212	10696392
10696419	10696853	10696896	10696906
10696921	10697312	10697450	10698160
10698223	10698785	10699230	10699562
10699670	10699708	10699757	10700231
10700338	10700412	10701002	10701224
10701252	10640401		

Revision History

Revision	Description
1.0	Initial Release