Quartus II Software Version 11.0 Release Notes

RN-01064-1.0 Release Notes

This document provides late-breaking information about the following areas of the Altera® Quartus® II software version 11.0:

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For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<*version number*>/quartus directory**. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Version 11.0 Device Support Release Notes*. For the latest information about the MegaCore® IP Library, refer to the *MegaCore IP Library Release Notes and Errata*. Both documents are available on the Altera website at http://www.altera.com/literature/lit-rn.jsp.

New Features & Enhancements

The Quartus II software version 11.0 includes the following new features and enhancements:

- Qsys, a system integration tool that captures system-level hardware designs and automates the task of defining and integrating custom HDL design blocks, IP cores, and components. During system generation, Qsys automatically creates high-performance interconnect logic from the connectivity you specify, eliminating the error-prone and time consuming task of manually writing HDL to specify the interconnect logic.

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- The Quartus II software version 11.0 includes the Deinterlacer II IP core.
- Analysis and Synthesis now includes design hierarchy elaboration without logic evaluation as a command-line option to the **quartus_map** executable.
- The Chip Planner now includes the required clock path for paths located from the TimeQuest Timing Analyzer, optionally displays the routing elements used to connect resources, and (for the Stratix V device family) improves the display of high-speed serial interfaces by distinguishing between receiver channels and transmitter channels in a logical data flow order.
- DSP Builder now supports 64-bit Windows and Linux operating systems.
- The Transceiver Toolkit delivers an improved channel manager interface and an updated transceiver control panel, helping you to optimize your transceivers for improved signal integrity and to bring up your boards faster.
- Quartus II Help can be used with the following browsers:
  - Local Quartus II Help (Help on a local drive installed by the Altera Installer) is fully compatible with Microsoft Internet Explorer 7 and Safari 4 running on Windows XP 32-bit operating systems. You can view the Quartus II Help in Google Chrome; however, you cannot open a Chrome browser from the Quartus II GUL. You must start Chrome with the `--allow-file-access-from-files flag` and then navigate to *<quartus installation directory>***/common/help/master.htm**.
  - Local Quartus II Help can be used with Mozilla Firefox 2.0 running on Linux systems and Mozilla 3.5 running on Windows systems; however, some Help text display controls are not functional.
  - Quartus II Web Help (hosted at http://quartushelp.altera.com/current) is fully compatible with Microsoft Internet Explorer 7, Safari 4, and Google Chrome.
  - Quartus II Web Help can be used with Mozilla Firefox; however, some Help text display controls are not functional.

EDA Interface Information

The Quartus II software version 11.0 supports the following EDA tools:

Synthesis Tools	Version	NativeLink Support
Synopsys Synplify, Synplify Pro, and Synplify Premier	E-2011.03	✓
Mentor Graphics® Precision RTL Synthesis	2010a	✓
Mentor Graphics LeonardoSpectrum™	2010a	✓
Mentor Graphics DK Design Suite	5.0 SP5	✓
Simulation Tools	**Version**	**NativeLink Support**
Mentor Graphics ModelSim®	6.6d	✓
Mentor Graphics ModelSim-Altera	6.6d	✓
Mentor Graphics ModelSim-Altera Starter Edition	6.6d	✓

Mentor Graphics QuestaSim	6.6d	✓
Cadence NC-Sim	9.2 (Linux only)	—
Synopsys VCS / VCS MX	2010.06-SP1 (Linux only)	✓
Aldec Active-HDL	8.3 (Windows only)	✓
Aldec Riviera-PRO	2010.10	✓
Formal Verification Tools (Equivalence Checking)	**Version**	**NativeLink Support**
Cadence Encounter Conformal	8.1	—
Chip Level Static Timing Analysis	**Version**	**NativeLink Support**
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	**Version**	**NativeLink Support**
Mentor Graphics TAU	—	—
Board Level Symbol/Pin-out Management	**Version**	**NativeLink Support**
Mentor Graphics I/O Designer	—	—

Changes to Software Behavior

This section documents instances in which the behavior and default settings of the Quartus II software have been changed from earlier releases of the software.

Refer to the Quartus II Default Settings File (**.qdf**), *<Quartus II installation directory>***/quartus/bin/assignment_defaults.qdf**, for a list of all the default assignment settings for the latest version of the Quartus II software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 11.0	
The RAM: 3-PORT megafunction is no longer available in the MegaWizard™ Plug-In Manager, beginning with the Quartus II software version 11.0. Although you cannot use the MegaWizard Plug-In Manager to create new RAM 3-PORT megafunctions, existing designs that contain RAM: 3-PORT megafunctions can be compiled with the Quartus II software version 11.0.	To create a 3-port RAM, use two RAM: 2-PORT megafunctions and connect their write ports.

Description	Workaround
Mentor Graphics ModelSim-Altera no longer converts VHDL files to VHDL-87.	—

The ALTLVDS_RX and ALTLVDS_TX megafunctions have been enhanced for designs that target the Stratix V device family. The precision of the input clock rate parameter has been increased.
If your design uses an ALTLVDS_RX or ALTLVDS_TX megafunction created in the Quartus II software version 10.1 SP1 or earlier, you must refresh the megafunction before compiling your design in the Quartus II software version 11.0. If you do not refresh the megafunction, compilation fails with errors similar to the following:
`Error: Could not place fractional PLL nios_bts_port_lvds_x17:hsma_lvds_i|nios_bts_port_lvds_x17_top:nios_bts_port_lvds_x17_top_i|nios_bts_port_core:nios_bts_port_core_i|serdes_rx_x17:serdes_rx_x17_inst|altlvds_rx:ALTLVDS_RX_component|serdes_rx_x17_lvds_rx:auto_generated|pll_sclk~FRACTIONAL_PLL`
`Error: Could not place I/O pad hsma_rx_d_p[7]`
	To refresh your megafunction, on the **Frequency/PLL settings** tab of the **Parameter Settings** page of the ALTLVDS_RX or ALTLVDS_TX MegaWizard Plug-In Manager, under **Specify input clock rate by**, select the appropriate value in the **clock frequency** box or in the **clock period** box and then regenerate the megafunction.

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 11.0	
Many tools within the Altera Complete Design Suite cannot parse directory paths that contain spaces. If you install the Altera Complete Design Suite to a path that contains a space, these tools do not function correctly.	During installation of the Altera Complete Design Suite (or any of its components), ensure that the installation path contains no spaces.
In the TimeQuest Timing Analyzer, the `rise_from_clock`, `rise_to_clock`, and `fall_to_clock` options of the `set_max_skew` constraint do not properly constrain the design.	Use the `from_clock` and `to_clock` options and use an explicit clock collection instead of "*". For example, use `[get_clocks *]` or `[all_clocks]` instead of "*".

If your design contains an Altera external memory interface IP core with UniPHY, simulation using Aldec Riviera-PRO versions 2010.10 or 2011.02 might fail with a message similar to the following:
`Fatal Error: The simulator process terminated unexpectedly.`
`Error: Simulation initialization failed.`
	Contact Aldec Inc. to obtain Aldec Riviera-PRO version 2011.06 or later.

In the MegaWizard Plug-In Manager, Resource Usage information is not available for the ALTFP_ATAN and ALTFP_SINCOS megafunctions.	—

Issue	Workaround
By default, the Assembler and the Time Quest Timing Analyzer run in parallel during full compilation. In rare circumstances, parallel compilation can cause the Time Quest Analyzer to fail with an internal error similar to the following: `Internal Error: Sub-system: QSTA, File: /quartus/Taoism/qsta/qsta_sta_interface.cpp, Line: 1189`	If you encounter this error, disable parallel compilation by adding the following line to your project's Quartus II Settings File (**.qsf**): `set_global_assignment -name FLOW_ENABLE_PARALLEL_MODULES Off` And then re-run timing analysis.
Encrypted Mentor Graphics ModelSim-specific simulation models provided with the Quartus II software version 11.0 cannot be read by ModelSim versions earlier than 6.6c	Upgrade to Mentor Graphics ModelSim version 6.6d.

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 11.0	
On computers that use the Microsoft Windows Vista operating system, the GUI panes on the left side of the main window might be too narrow to display their information in the Quartus II software window with the Compilation Report open, the State Machine Editor window, and the TimeQuest Timing Analyzer window.	Adjust the width of the left pane, if necessary.
If you uninstall the Quartus II software version 11.0, some desktop shortcuts might not be fully removed.	Manually remove the remaining desktop shortcuts.
IP cores that use UniPHY use the NIOS II toolchain, which requires the proper registration of Cygwin. If you use the MegaWizard Plug-In Manager to generate Memory Controller IP cores that use UniPHY without first launching a tool that registers Cygwin (Qsys, SOPC Builder, or the NIOS II Software Build Tools), Analysis and Synthesis of the generated core can fail with errors similar to the following: `Error: Node instance "sequencer_ram" instantiates undefined entity "core1_example_if0_p0_qsys_sequencer_sequencer_ram"` Analysis and Synthesis can also fail if you install Altera Complete Design Suite version 11.0 tools in one directory, and then reinstall them in a different directory, or if you use different paths on a network installation.	If you have used the MegaWizard Plug-In Manager without having launched a tool that registers Cygwin, force proper registration of Cygwin, by running: `"$QUARTUS_ROOTDIR/bin/qreg.exe -force"`

Linux Platforms Only

Issue	Workaround
Version 11.0	
If your Linux operating system uses the X protocol C-language Binding (XCB) library (libxcb), the Quartus II software might fail to start with an error similar to the following: `quartus: xcb_xlib.c:82:xcb_xlib_unlock: Assertion 'c->xlib.lock' failed.`	Upgrade you Linux distribution to the latest version or, if your Linux distribution uses libxcb version 1.1, run `export LIBXCB_ALLOW_SLOPPY_LOCK=1` before running the Quartus II software version 11.0.
On computers that use the Red Hat Enterprise version 4 or Red Hat Enterprise version 5 operating systems, the shortcut key Ctrl+H is not available for the **Replace** command on the Edit menu of the main Quartus II software window.	To use the **Replace** command, click **Replace** on the Edit menu.
If you attempt to uninstall the Altera Complete Design Suite, but the current login account does not have sufficient permissions, uninstallation fails with the message: `TypeError: not enough arguments for format string.`	Use the same account to uninstall the software as was used to install the software. Ensure that the account has sufficient permissions to uninstall the software.

If, when using the Quartus II Web Edition software version 11.0, you start the Nios II command shell with the command
`nios2_command_shell.sh`
the Quartus II Web Edition software generates an error similar to the following:
`***The Quartus II software cannot be started because the current platform, 'linux64' does not appear to be installed in: '/home/sqa/altera/11.0a/quartus'.`
	You may safely ignore this message. The Nios II software starts and continues to work as expected.

Issue	Workaround
If you use the VHDL simulation models for DDR1-, DDR2-, or DDR3-based IP cores with the Aldec Riviera-PRO software version 2010.10, during simulation the Aldec Riviera-PRO software might generate an error similar to the following: `# KERNEL: FAILURE: 32-bit argument is too wide for CONV_INTEGER. Use `asim -relax' to allow 32-bit arguments for CONV_INTEGER`	Use the `-relax` option with the `asim` command.
If you use the MegaWizard Plug-In Manager to create two or more IP variations in your design, simulation of the design with Synopsys VCS / VCS MX fails with an error similar to the following: `Error-[MPD] Module previously declared` The file set for simulating your entire design contains duplicate files. This duplication may occur if your design has multiple variations of the same IP core, or if different IP cores share some simulation files (for example, SystemVerilog packages common to multiple IP cores). For some IP cores, during IP file generation of an IP variation, a complete simulation file set is added to the *<variation>*_**sim directory**. Each variation's file set includes copies of all the IP simulation model files required to simulate the variation, including some files that may be shared with other IP cores. The concatenated list of all simulation files names for all IP variations (including the duplicate filenames) that is added to the VCS command line causes the error. NOTE: The file set does not include copies of the simulation library files that are installed in the **quartus/eda/sim_lib** directory and directories below it.	Refer to the solution available at http://www.altera.com/support/kdb/solutions/rd05172011_198.html.

Device Family Issues

Arria II GX

Issue	Workaround
Version 11.0	
If, in the ALTGX MegaWizard Plug-In Manager, you set **Which protocol will you be using?** to **Deterministic Latency** on the **General** tab of the **Parameter Settings** page, the MegaWizard Plug-In Manager does not automatically update the voltage output differential (VOD) settings on the **Tx Analog** tab.	To update the two VOD settings (**What is the voltage output differential (VOD) control setting?** and **What is the Pre-emphasis setting (% of VOD)?**), on the **Tx Analog** tab, select **150 Ohms** in the **Select the Transmitter termination resistance** box.

During simulation of a Qsys-generated VHDL design that includes DDR2 or DDR3 external memory cores with ALTMEMPHY, the 64-bit version of Mentor Graphics ModelSim SE 6.6d may issue a fatal error similar to the following:
`#**Note: (vsim-3812) Design is being optimized...`
`#**Fatal: Unexpected signal: 11.`
	Use the 32-bit version of Mentor Graphics ModelSim SE 6.6d or use the `-novopt` option with the `vsim` command.

Cyclone III LS

Issue	Workaround
Version 11.0	
If you use the **Convert Programming Files** dialog box to regenerate a Hexadecimal (Intel-Format) Output File (**.hexout**) the generated file might contain incorrect option register and start addresses if you changed these values from those used during the previous generation.	Use the **quartus_cbf.exe** command line executable to regenerate the **.hexout** file, or close and then reopen the **Convert Programming Files** dialog box before regenerating the file.

Cyclone IV GX

Issue	Workaround
Version 11.0	
Although you can generate an SDI megafunction with the MegaWizard Plug-In Manager, Cyclone IV GX EP4CGX15, EP4CGX22, and EP4CGX30 devices (except EP4CGX30F484) do not support the HD-SDI and HD-SDI 3G video standards. The behavior of an SDI megafunction that uses the HD-SDI or HD-SDI 3G video standard in these devices is untested and unreliable.	Use EP4CGX30F484, EP4CGX75, EP4CGX110, or EP4CGX150 devices for HD-SDI and HD-SDI 3G.
In the ALTGX MegaWizard Plug-In Manager, the **rx_seriallbken**, **tx_pipedeemph**, **tx_pipemargin**, and `tx_pipeswing` ports are not supported. If you enable any of these ports, compilation fails with the following message: `Error: Port "<port name>" does not exist in macrofunction "basic_alt_c3gxb_component"`	Do not enable any of these ports.

MAX V

Issue	Workaround
Version 11.0	

In the MegaWizard Plug-In Manager for the ALTUFM_I2C, ALTUFM_NONE, ALTUFM_PARALLEL, and ALTUFM_SPI megafunctions, the options listed in the **Oscillator frequency** box on the **Parameter Settings** page are incorrect. The incorrect options listed are **5.56 MHz** and **3.33 MHz**. They should be **5.3 MHz** and **3.9 MHz**.	Use clearbox commands to set **Oscillator frequency** to a valid value.
	For Verilog HDL designs:
	■ To set **Oscillator frequency** to **5.3 MHz**, use the command
	`clearbox cbx_altufm_osc OSC_FREQUENCY=188679 osc oscena DEVICE_FAMILY="MAX V" cbx_file=ufmosc.v`
	■ To set **Oscillator frequency** to **3.9 MHz**, use the command
	`clearbox cbx_altufm_osc OSC_FREQUENCY=256410 osc oscena DEVICE_FAMILY="MAX V" cbx_file=ufmosc.v`
	For VHDL designs:
	■ To set **Oscillator frequency** to **5.3 MHz**, use the command
	`clearbox cbx_altufm_osc OSC_FREQUENCY=188679 osc oscena DEVICE_FAMILY="MAX V" cbx_file=ufmosc.vhd`
	■ To set **Oscillator frequency** to **3.9 MHz**, use the command
	`clearbox cbx_altufm_osc OSC_FREQUENCY=256410 osc oscena DEVICE_FAMILY="MAX V" cbx_file=ufmosc.vhd`

Stratix III

Issue	Workaround
Version 11.0	

During simulation of a Qsys-generated VHDL design that includes DDR2 or DDR3 external memory cores with ALTMEMPHY, the 64-bit version of Mentor Graphics ModelSim SE 6.6d may issue a fatal error similar to the following:
`#**Note: (vsim-3812) Design is being optimized...`
`#**Fatal: Unexpected signal: 11.`
	Use the 32-bit version of Mentor Graphics ModelSim SE 6.6d or use the `-novopt` option with the `vsim` command.

Stratix IV GX

Issue	Workaround
Version 11.0	
In the ALTGX MegaWizard Plug-In Manager, the **Receiver only** option is unavailable in the **What is the operation mode?** box on the **General tab** of the **Parameter Settings** page.	To make the **Receiver only** option available, follow these steps: 1.In the **Which subprotocol will you be using?** box, select **XN**. 2.In the **Which subprotocol will you be using?** box, select **None**. The **Receiver only** option in the **What is the operation mode?** box is now available.
In the ALTGX MegaWizard Plug-In Manager, if on the **General** tab of the **Parameter Settings** page, you set **What protocol will you be using?** to **Basic (PMA Direct)** and **Which subprotocol will you be using?** to **None**, and on the **PLL/Ports** tab, you turn on **Auxiliary Transmitter (ATX) PLL**, elaboration fails.	To use an ATX PLL with the Basic (PMA Direct) protocol, set **Which subprotocol will you be using?** to **XN**.

Stratix V

Issue	Workaround
Version 11.0	
Any top or bottom central PLL in Stratix V ES devices that has its reference clock fed by a clock network should not be fed a clock faster than 400 MHz.	If possible, directly feed the reference clock from a pin or manually place the PLL on the left or right side.

Due to a problem in the ModelSim-Altera Starter Edition software version 6.6c and 6.6d, designs in VHDL that target Stratix V devices cannot be simulated. This problem does not affect the ModelSim-Altera Edition software.
Due to this problem, you may see errors similar to the following:
`# ALTERA version supports only a single HDL`
`# ** Fatal: (vsim-3512) Instantiation of 'stratixv_ds_coef_sel' failed. Unable to check out Verilog simulation license.`
	Simulate the design with Verilog HDL or use the ModelSim-Altera Edition software version 6.6d.

In the Cadence NC-Sim software, if you attempt to perform, using **altera_lnsim.sv**, RTL simulation of a VHDL design that contains an ALTMULT_ADD megafunction, the NC-Sim software issues the following error: `ncelab: *F,GENPAR: VHDL generic ALTERA_MULT_ADD.ACCUM_DIRECTION (./cplxmult.vhd: line 65, position 16) and verilog parameter being overridden altera_mult_add.extra_latency (/tools/acdskit/11.0/140/linux64/quartus/eda/sim_lib/altera_lnsim.sv: line 3631, position 23) are not type compatible.`	To prevent the error, use the `-namemap_mixgen` option with the **ncelab** command.

Issue	Workaround
Pre- and post-configuration Boundary-Scan Description Language Files (**.bsd**) generated by the Quartus II software omit a ground pin. During generation of a **.bsd** file, a Boundary-Scan Description Language syntax error is not displayed for this omission.	Download a correct pre-configuration Stratix V **.bsd** file from the Altera BSDL Support page on the Altera website.
User mode on-chip termination (OCT) calibration is not available in the ALT_OCT megafunction.	Use power-up mode OCT calibration.
EDGE_BOTTOM, EDGE_LEFT, EDGE_RIGHT, and EDGE_TOP pin **Location** assignment options are not available in the Quartus II software version 11.0.	Make pin assignments to specific locations.
Any top or bottom central PLL in Stratix V ES devices that has its reference clock fed by a clock network should not be fed a clock faster than 400 MHz.	If possible, directly feed the reference clock from a pin or manually place the PLL on the left or right side.
In the Cadence NC-Sim software, if you attempt to perform, using **altera_lnsim.sv**, RTL simulation of a VHDL design that contains an ALTMULT_ADD megafunction, the NC-Sim software issues the following error: `ncelab: *F,GENPAR: VHDL generic ALTERA_MULT_ADD.ACCUM_DIRECTION (./cplxmult.vhd: line 65, position 16) and verilog parameter being overridden altera_mult_add.extra_latency (/tools/acdskit/11.0/140/linux64/quartus/eda/sim_lib/altera_lnsim.sv: line 3631, position 23) are not type compatible.`	To prevent the error, use the `-namemap_mixgen` option with the **ncelab** command.
Pre- and post-configuration Boundary-Scan Description Language Files (**.bsd**) generated by the Quartus II software omit a ground pin. During generation of a **.bsd** file, a Boundary-Scan Description Language syntax error is not displayed for this omission.	Download a correct pre-configuration Stratix V **.bsd** file from the Altera BSDL Support page on the Altera website.
User mode on-chip termination (OCT) calibration is not available in the ALT_OCT megafunction.	Use power-up mode OCT calibration.
EDGE_BOTTOM, EDGE_LEFT, EDGE_RIGHT, and EDGE_TOP pin **Location** assignment options are not available in the Quartus II software version 11.0.	Make pin assignments to specific locations.
Quartus II Incremental Compilation in the Quartus II software version 11.0 has some limitations regarding the merging and processing of high-speed serial interface (HSSI) atoms. Placing transceivers from different partitions into the same triplet requires the transceivers to share reconfiguration logic. Partition legality checks prevent the Fitter from merging that reconfiguration logic—if the device has enough transceiver locations available, the Fitter can use a second triplet; however, if not enough locations are available, the lack of triplets can cause a no-fit with the following error: `Error: Partition assignments may be preventing transceiver placement-transceiver optimizations across partitions are not supported in this version of the Quartus II software.`	Remove or modify partition assignments on hierarchies containing transceiver logic so that the transceivers and reconfiguration logic that should be placed in the same triplet are in the same partition.

Issue	Workaround
Quartus II Incremental Compilation in the Quartus II software version 11.0 has some limitations regarding the merging and processing of RAMs into RAM blocks. If your design includes post-fit partition that contains a Transceiver Reconfiguration Block (**alt_xcvr_reconfig**) connected to a Transceiver PHY IP core and that Transceiver PHY IP core contains an Avalon Memory Map block, Place and Route might fail with an error similar to the following: `Error: Fitter was not able to process memory blocks within the Transceiver Reconfiguration Controller (alt_xcvr_reconfig) connected to a XCVR PHY IP containing component Avalon Memory Map block <Avalon Memory Map block name>.`	Ensure that the Transceiver Reconfiguration Controller is not placed in a post-fit Quartus II Incremental Compilation partition.

If you apply both a FAST_INPUT_REGISTER assignment to an I/O and a D3_DELAY assignment to the associated delay chain, compilation might fail with an error similar to the following:
`Error: Can't route signal "in~input" to atom "io_ff"`
`Error: Can't fit design in device`
	Do not apply both a D3_DELAY assignment and a FAST_INPUT_REGISTER assignment. You may safely apply either assignment, but not both.

The PowerPlay Early Power Estimator File (**.csv**) generated by the Quartus II software does not contain any transceiver or FFPLL information. During generation, the Quartus II software displays the following message: `Info: PowerPlay Early Power Estimator (EPE) File will not contain any HSSI related information for the device family Stratix V`	—
If you compile a design that uses the **Differential 1.2-V HSUL** standard, compilation fails with the error: `Internal Error: Sub-system: FSV, File: /quartus/fitter/fsv/fsv_module_oct.cpp, Line: 653 too many OCTs`	Review the number of calibration blocks required by your design, and merge them using the TERMINATION_CONTROL_BLOCK assignment.

If you attempt to simulate, using the Mentor Graphics ModelSim-Altera software, a VHDL design that contains a Low Latency PHY megafunction with a 10 Gbps datapath, simulation fails with errors similar to the following:
`# ** Fatal: Error occurred in protected context.`
`#  Time: 0 ps  Iteration: 0  Instance: /test_tst/test_inst/test_inst/<protected>/<protected>/<protected> File: nofile`
`# FATAL ERROR while loading design`
`# Error loading design`
	—

If you attempt to use the Cadence Encounter Conformal software for formal verification of **altddio_out.v**, **altlvds_tx.v**, **altlvds_rx.v**, **lvds_tx.v**, **lvds_rx.v**, **flvds_tx.v**, **flvds_rx.v**, **altmult_add.v**, **altmult_accum.v**, or **altpll.v**, formal verification fails with the error: `Error RTL 18.3: Function call does not refer to function definition`	—

SOPC Builder Issues

Issue	Workaround
Version 11.0	
If you attempt to update an SOPC Builder system that uses **altera_avalon_clock_source** bus functional model (BFM) from the Quartus II software version 10.1 to the Quartus II software version 11.0, the system cannot be opened.	In SOPC Builder version 11.0, add the 10.1 version of the component to the search path and explicitly use only the 10.1 version with SOPC Builder.
Failure to assign, on each slave mastered by an Avalon Memory-Mapped (Avalon-MM) interface that controls arbitration locking with lock role, an **Arbitration Priority** of **1** to the Avalon-MM interface can result in unpredictable interconnect behavior, including failure to lock arbitration, lost data, and interconnect lockup.	On every slave that the interface masters, set **Arbitration Priority** to **1** for the Avalon-MM interface that controls arbitration locking with lock role.
Some configurations synchronous resets are not supported by SOPC Builder. If any of the following conditions are met, the HDL that SOPC Builder generates fails to connect reset ports: ■ The reset port is not associated with a clock. ■ The reset port is an output and no Avalon interface (master or slave) exists on the same clock domain. ■ The reset port is an input and its associated clock is an output. No validation or generation messages are displayed.	To confirm that a reset port is not connected, do the following: 1. Open the top-level design file generated by SOPC Builder in a text editor. (The top-level design file has a file name equal to the system name and a file extension corresponding to the HDL language you chose for system generation.) 2. Inspect the instantiation of each module. For a given module named X in the SOPC Builder system, a module/entity named X is instantiated in the top-level design file. In the module/entity instantiation, the ports are connected by name. If any of the conditions listed in the Issue description are met, the reset signal is not connected to the global reset bus. If you find an unconnected reset port, do one of the following: 1. Use the Qsys Editor. On the Tools menu of the main Quartus II window, click **Qsys** and then open the SOPC Builder Design File (**.sopc**) and convert your system to Qsys. 2. Manually modify the HDL to connect the reset. If the reset is expected to be synchronized, you must also manually implement synchronization. Reset synchronizers have a module name that consists of *<SOPC system name>*_reset_*<externally driven clock name>*_domain_synch_module. For example, an SOPC system named sys with a clock source named `clk_0` has a reset synchronizer module named sys_reset_clk_0_domain_synch_module. A reset synchronizer, for example, is generated for an external clock source in your SOPC system.

Issue	Workaround
When you add new components created with the Component Editor to SOPC Builder systems, SOPC Builder might generate errors similar to the following: `Error: <component name>: TOP_LEVEL_MODULE not specified, file <file name> contained multiple modules`	In the **hw.tcl** file for the component, remove the line that starts with: `set_module_property STATIC_TOP_LEVEL_MODULE_NAME` and then refresh the library or restart SOPC Builder.
For some Stratix V block types, the TimeQuest Timing Analyzer might report recovery and removal timing for clear and asynchronous reset signals in the Setup Summary report and the Hold Summary report, instead of in the Recovery Summary report and the Removal Summary report. The affected block types are: ■ M20K ■ LAB ■ READ_FIFO ■ HSSI_8G_TX_PCS ■ HSSI_8G_RX_PCS ■ HSSI_10G_TX_PCS ■ HSSI_10G_RX_PCS	To view recovery and removal timing data for these blocks, look in the setup and hold reports.

Qsys Issues

Issue	Workaround
Version 11.0	
If you use Qsys to generate a Block Symbol File (**.bsf**) for schematic design entry, the ports of the generated symbol may appear in any order. The order of the ports might change if you regenerate the file.	If you use a schematic to instantiate your Qsys system, you must regenerate a **.bsf** symbol and reconnect the signals in the Block Diagram File (**.bdf**) each time you change the top-level signals of your Qsys system. If you do not change the top-level signals of the Qsys system, you can turn off symbol generation and reuse the previously generated symbol in your **.bdf**. Alternatively, use a VHDL or Verilog top-level design file to instantiate your Qsys system.
Slaves wider than the master might receive illegal byteenable combinations during burst transactions.	Ensure that the bursting master performs accesses aligned to the slave word size. For example, if a 32-bit master accesses a 128-bit slave, ensure that the master accesses offsets in the slave address space that are multiples of 16 bytes.

Issue	Workaround

Qsys does not support the following Avalon Memory-Mapped (Avalon-MM) flow control signals: `dataavailable`, `readyfordata`, `endofpacket`, and `flush`.
For components that use the deprecated Memory-Mapped flow control, Qsys issues warnings during generation. For the Altera Avalon JTAG UART and DMA Controller components, Qsys generates messages similar to the following:
`Warning: "No matching role found for jtag_uart_0:avalon_jtag_slave:dataavailable (dataavailable)"`
`Warning: "No matching role found for dma_0:read_master:read_flush (flush)"`
	You may safely ignore these messages for Altera components because the signals are not required for design operation.
	If generation of a Qsys system produces similar messages for a custom component or IP block, check with the custom component or IP block author to ensure that the signals listed are not required.

Qsys does not support components that have the module property `INSTANTIATE_IN_SYSTEM_MODULE` set to `FALSE`. Qsys does not export to the top-level interfaces of components that are not instantiated in the system to the top level.	To manually export the interface of a module that is not instantiated in Qsys to the top level: 1. Create a wrapper HDL file. 2. Map one half of the wrapper to Avalon-compliant interfaces, and the other half to a conduit. 3. Manually export the conduit by specifying the exported name in the **Export As** column in Qsys.
If you instantiate a Qsys system within the same Qsys system, Qsys fails with unexpected behavior.	Recursive nesting of Qsys systems is not supported.
Connecting a tristate conduit pin sharer output interface to its input interface causes the GUI to become unresponsive.	You cannot connect a tristate conduit pin sharer to itself.
Quartus II Archive Files (**.qar**) do not automatically include Qsys input files such as Qsys System Files (**.qsys**) and the source files for custom components defined in the system.	To include the Qsys input files in the **.qar** file, in the **Archive Project** dialog box, click **Advanced**, then click **Add**, and then browse to the files.
Interrupt bridges are not supported by the Nios II Embedded Design Suite Board Support Package (BSP) tools. If interrupt requests (IRQs) are mapped for a module to a CPU interrupt receiver port, the BSP tools publish incorrect information to the **system.h** file. IRQ IDs appear in the file with a value of `-1`.	Using the information in the Qsys system IRQ map, create a set of `#define` statements in a new Header File (**.h**). Because a BSP tool can overwrite the **system.h** file during generation, do not edit the **system.h** file.
If a Qsys component interface is exported by default, the name of the exported interface is based on the original instance name—the exported interface names are *not* renamed if you edit the instance name.	To update the name of the exported interface (and the associated input and output signals of the system), click in the **Export** column and then rename the interface.
You can directly connect a maximum of 32 slaves connected to a master.	If you need to connect more than 32 slaves, use pipeline bridges to reduce the number of slaves that are directly connected to a master.
If you disable an instance in Qsys and then add a new instance with the same name and interfaces, duplicate connections might be created, resulting in an incorrect interconnect.	Remove the instance (instead of disabling it) before adding an instance with the same name.

Issue	Workaround
The clock period of an Altera Avalon Clock Source bus functional model (BFM) generated by Qsys is not accurate. If you set up your design with the default clock source and then generate the testbench Qsys system and testbench simulation model, the generated testbench Qsys system uses the Altera Avalon Clock Source BFM (altera_avalon_clock_source) as the clock's source.	To correct the clock period: 1. Open the generated **altera_avalon_clock_source.sv** file in *<Qsys output directory>***/simulation/submodules**. 2. Change `'timescale 1ns/1ns` to `'timescale 1ns/1ps`. If you require a smaller time unit, use `'timescale 1ns/1fs`. 3. Change `localparam CLOCK_PERIOD = 1000/CLOCK_RATE;` to `localparam CLOCK_PERIOD = 1000.000000/CLOCK_RATE;`.
If you create a new system and save it to a different directory from the original project directory, the generation paths remain set to the original project directory, even if Qsys is restarted.	To correct the generation paths, delete the **Path** box in the **Generation** tab and press Enter. Qsys automatically populates the field with the correct generation path.
When you add new components created using the Component Editor to Qsys systems, Qsys might generate errors similar to the following: `Error: <component name>: TOP_LEVEL_MODULE not specified, file <file name> contained multiple modules`	In the **hw.tcl** file for the component, remove the line that starts with: `set_module_property STATIC_TOP_LEVEL_MODULE_NAME` and then refresh the library or restart Qsys.
Qsys does not support legacy SOPC Builder PLL components, except those with an input frequency of 50 MHz. Generating a design that includes a legacy PLL with an input frequency not set to 50 MHz fails with an error similar to the following: `Error: altera_avalon_pll_khh3cm2h: CLock yyclock_inclk0 of frequency 50.000 MHz driving the PLL module conflicts with the PLL inclock of frequency 125.000 MHz.`	If you want to configure a PLL with an input frequency other than 50 MHz, replace the SOPC Builder PLL with an Avalon ALTPLL.
The Avalon-MM `arbiterlock` signal is not supported.	For all Avalon-MM masters that use `arbiterlock`, add burst capabilities to the master and set the burst count according to the duration of arbiter lock required. For example, replace an arbiter locked transaction of 16 accesses with a burst transaction using a burst count of 16.
If an Avalon Memory-Mapped (MM) master writes to an Avalon-MM slave that does not have a byte enable input signal and has a wider data width than the master, data corruption might occur on the slave words.	Add a byte enable signal to any slave that has a wider data width than its master.
When converting an SOPC Builder system with more than one clock source to Qsys, the generated Qsys system has multiple reset inputs—one for each clock source.	In the top level of your design, connect all reset inputs generated by Qsys to the same reset source.
If your system includes multiple reset sources, a transaction can be issued from a component in a reset domain that is not currently reset to a domain that is currently in reset. The transaction might be accepted by the interconnect logic within the domain that is currently in reset. The result is system-dependent, but can include system lockup—the transaction appears to have been accepted, but actually is ignored.	Carefully control reset deassertion sequencing among multiple reset domains and ensure that transactions are not issued across reset domain boundaries when some reset domains are in reset but others are not in reset. You can also use the **Create Global Reset Network** command on the System menu to connect all reset signals.

IP Issues in Qsys

Issue	Workaround
Version 11.0	
Not all Altera IP megafunctions support Qsys. For example, Qsys does not include the 10GBASE-R PHY, ASI, CPRI, FFT, FIR COMPILER, VITERBI, and XAUI PHY megafunctions.	Use the MegaWizard Plug-In Manager for these functions. For a complete list of IP megafunctions available in Qsys, refer to the **Component Library** tab in the Qsys GUI.
For Qsys designs that include a Triple Speed Ethernet (TSE) MegaCore function and target the Cyclone IV GX device family, Synopsys Design Constraint Files (**.sdc**) generated by Qsys contain the following warning: `Warning: ignored filter at altera_reset_controller.sdc(17): *|alt_rst_sync_uq1|altera_reset_synchronizer_int_chain*|aclr could not be matched with a pin`	This warning does not pertain to the Cyclone IV GX device family and is generated in error. You may safely ignore this warning.

If a Qsys system that contains IP cores such as ALTPLL or a UniPHY component has any disconnected interfaces at generation time, Qsys issues errors similar to the following, even if the interfaces are optional:
`Warning: top_system.sdram: sdram.status must be exported, or connected to a matching conduit.`
`Warning: top_system.sdram: sdram.local_powerdown must be exported, or connected to a matching conduit.`
	Check with the component or IP author to verify whether the interfaces listed in the errors are not required. You can safely ignore these warnings if the interfaces are optional. If they are not optional, connect the interfaces.

Qsys does not give a clear warning that an OCT interface of a component using UniPHY cannot be connected internally.	If you unexport the OCT interface of a component with UniPHY, you must export and externally connect it to have a working design.
If an SSRAM controller is driven by a clock that is phase-shifted from the clock that drives the memory model in the testbench, during simulation the SSRAM memory model might not function correctly.	Drive the SSRAM controller with a clock that has zero phase-shift from the memory model's clock.
For designs that include ALTMEMPHY, the *<memory controller name>*_**pin_assignments.tcl** file generated by Qsys does not assign correct pin names. Running the Tcl file immediately after generation might result in incorrect pin assignments.	After you generate your design and before you run the Tcl script, open the Tcl file and verify that the `${pin_prefiix}` varaiable is set correctly to match the Qsys prefix to the memory I/O signals of your Qsys system (for example, *<exported interface name>*`_mem_`).
If you simulate an ALTMEMPHY-based megafunction as part of a Qsys system, the simulator might generate the following error: `Instantiation of 'stratixiii_ddio_in' failed`	Add the following global assignment to the Quartus II IP File (**.qip**) generated by Qsys: `set_global_assignment -name EDA_DESIGN_EXTRA_ALTERA_SM_LIB stratixiii -section_id eda_simulation`
Qsys does not support the **Controller shares dq/dqm/addr I/O pins** option of the SDRAM Controller. Attempting to use an SDRAM Controller with **Controller shares dq/dqm/addr I/O pins** turned on results in an error similar to the following: `Error: sdram_0: Invalid tristate bridge selection for pin-sharing. Please parameterize the SDRAM to resolve this issue.`	On the **Memory Profile** page of the **Parameter Settings** tab of the SDRAM Controller Parameter Editor, turn off **Controller shares dq/dqm/addr I/O pins**.

Antivirus Verification

The Altera Complete Design Suite version 11.0 has been verified virus free using the following software:

AVG Version 10.0.1209
Virus database version: 1500/3533

McAfee VirusScan Enterprise + AntiSpyware Enterprise 8.7.0i
Scan Engine Version: 5400.1158
DAT Version: 6312.0000

Panda Antivirus Pro 2011 version 10.00.00

Latest Known Quartus II Software Issues

For more information about known software issues, look for information on the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

For the latest known issues related to Qsys, refer to the New Qsys Issues wiki page at the following URL:

http://www.alterawiki.com/wiki/New_Qsys_Issues

You can find known issue information for previous versions of the Quartus II software on the Knowledge Database page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Quartus II software version 11.0:

Customer Service Request Numbers Resolved in the Quartus II Software Version 11.0							
10006605	10587477	10606225	10626214	10629510	10631310	10642540	10645012
10647230	10647985	10655044	10656999	10658415	10663928	10670495	10673097
10678329	10679715	10683347	10690220	10691877	10696419	10697716	10697904
10700610	10704712	10705736	10707177	10709335	10709526	10709681	10710082
10710136	10711675	10716315	10718129	10718766	10719884	10721149	10721345
10723252	10725380	10727706	10729604	10730625	10731214	10731939	10733274
10734026	10734030	10734060	10734803	10734958	10734971	10735439	10735750
10736214	10737187	10737399	10737780	10738094	10738118	10738596	10739620
10740189	10740245	10740857	10741378	10742139	10742258	10742717	10743006
10744019	10745086	10745167	10745321	10745902	10746196	10746730	10746779
10749372	10750340	10750750	10750780	10751053	10751208	10751279	10751703
10751783	10753031	10753183	10753383	10753942	10753969	10754061	10754065
10754093	10754676	10754945	10755335	10756722	10757176	10757248	10757366
10757551	10758193	10758519	10758718	10759155	10759553	10759816	10759939
10760191	10760519	10761181	10761688	10762758	10763013	10764949	10765067

Customer Service Request Numbers Resolved in the Quartus II Software Version 11.0							
10765151	10766811	10767444	10767623	10767660	10767838	10768209	10768237
10768309	10768413	10768765	10768778	10768973	10769054	10769576	10769865
10769961	10769964	10770015	10770017	10770061	10770313	10770328	10770523
10770859	10771051	10771288	10771435	10771600	10771753	10771996	10772027
10772034	10772523	10772715	10772722	10772918	10773384	10773416	10773578
10773686	10773974	10774581	10774655	10774806	10774811	10775162	10775350
10775351	10775608	10776173	10776228	10776244	10776316	10776331	10776570
10776682	10776708	10776975	10777263	10777301	10777503	10777629	10777767
10777784	10777955	10777984	10778025	10778039	10778287	10778509	10778682
10778844	10778944	10778998	10779044	10779238	10779250	10779281	10779387
10779431	10779464	10779721	10779781	10779821	10780185	10780214	10780248
10780326	10780353	10780413	10780414	10780520	10780552	10780652	10780691
10780813	10780839	10780889	10780940	10780980	10780993	10781007	10781024
10781078	10781087	10781153	10781197	10781356	10781450	10781509	10781548
10781860	10781956	10782080	10782098	10782120	10782397	10782419	10782429
10782588	10782652	10782801	10782827	10782938	10783043	10783129	10783280
10783282	10783292	10783365	10783417	10783428	10783473	10783478	10783484
10783500	10783515	10783585	10783717	10783982	10783988	10783995	10784093
10784173	10784239	10784243	10784248	10784253	10784277	10784278	10784471
10784543	10784554	10784605	10784666	10784674	10784695	10784741	10784743
10784848	10784993	10785063	10785115	10785159	10785237	10785268	10785292
10785300	10785307	10785334	10785484	10785613	10785755	10785836	10786012
10786044	10786220	10786231	10786269	10786290	10786310	10786325	10786380
10786432	10786435	10786468	10786528	10786585	10786588	10786598	10786614
10786637	10786655	10786662	10786690	10786693	10786742	10786766	10786785
10786814	10786825	10786878	10786917	10786996	10787243	10787255	10787264
10787387	10787440	10787586	10787627	10787640	10787661	10787721	10787808
10787923	10787965	10787997	10788044	10788116	10788171	10788173	10788185
10788193	10788213	10788232	10788265	10788308	10788314	10788330	10788343
10788389	10788473	10788600	10788626	10788657	10788661	10788670	10788780
10788983	10789114	10789196	10789202	10789355	10789356	10789386	10789548
10789571	10789577	10789783	10789875	10789946	10789972	10790022	10790089
10790175	10790181	10790334	10790346	10790353	10790389	10790397	10790411
10790446	10790470	10790491	10790503	10790514	10790536	10790565	10790579
10790595	10790641	10790711	10790717	10790726	10790750	10790827	10790840
10790891	10790904	10790913	10790919	10790920	10791024	10791100	10791129
10791214	10791299	10791303	10791320	10791335	10791353	10791394	10791442
10791548	10791581	10791619	10791711	10791759	10791795	10791949	10791962
10791970	10792010	10792138	10792176	10792199	10792226	10792241	10792250
10792265	10792292	10792362	10792377	10792381	10792402	10792420	10792425

Customer Service Request Numbers Resolved in the Quartus II Software Version 11.0							
10792426	10792443	10792485	10792514	10792527	10792563	10792591	10792592
10792594	10792600	10792601	10792625	10792754	10792860	10792891	10792943
10793047	10793065	10793084	10793173	10793177	10793197	10793279	10793321
10793329	10793373	10793413	10793494	10793504	10793530	10793579	10793681
10793741	10793768	10793772	10793782	10793831	10793860	10793865	10793890
10793910	10793923	10793950	10793958	10793977	10793994	10794031	10794033
10794035	10794042	10794044	10794097	10794114	10794121	10794218	10794299
10794311	10794318	10794334	10794528	10794543	10794590	10794677	10794681
10794792	10794801	10794805	10794823	10794835	10794848	10794989	10794997
10795009	10795022	10795058	10795081	10795119	10795226	10795289	10795301
10795312	10795443	10795468	10795491	10795511	10795597	10795672	10795683
10795706	10795719	10795722	10795756	10795778	10795828	10795861	10795999
10796077	10796082	10796101	10796158	10796185	10796236	10796288	10796291
10796320	10796379	10796531	10796546	10796556	10796584	10796595	10796659
10796664	10796688	10796855	10796863	10796944	10797072	10797088	10797120
10797229	10797322	10797324	10797339	10797368	10797371	10797391	10797400
10797489	10797514	10797573	10797594	10797641	10797665	10797718	10797757
10797886	10797953	10798012	10798116	10798159	10798226	10798228	10798256
10798301	10798478	10798525	10798592	10798602	10798603	10798621	10798638
10798650	10798681	10798698	10798707	10798762	10798774	10798794	10798817
10798908	10798927	10798943	10799098	10799102	10799105	10799126	10799180
10799200	10799277	10799279	10799292	10799303	10799343	10799393	10799437
10799484	10799492	10799630	10799675	10799686	10799696	10799783	10799785
10799906	10799938	10799995	10800053	10800060	10800088	10800370	10800463
10800468	10800507	10800513	10800567	10800576	10800687	10800930	10801056
10801424	10801482	10801499	10801526	10801602	10801770	10801777	10801887
10801898	10801935	10801963	10802036	10802043	10802055	10802081	10802085
10802208	10802326	10802356	10802379	10802471	10802499	10802620	10802667
10802683	10802702	10802871	10802880	10802886	10802904	10803038	10803139
10803263	10803269	10803277	10803327	10803343	10803431	10803499	10803516
10803518	10803647	10803650	10803790	10803805	10803886	10803906	10803926
10804048	10804059	10804067	10804071	10804156	10804198	10804569	10804692
10804693	10804764	10804838	10804889	10805014	10805467	10805561	10805614
10805739	10805869	10806015	10806116	10806181	10806182	10806312	10806857
10806956	10807086	10808035	10809554	10809770	—	—	—

Software Patches Included in this Release

The Quartus II software version 11.0 includes the following patches released for previous versions of the Quartus II software:

Quartus II Software Version	Patch	Customer Service Request Number
10.1 SP1	1.62	10808195
10.1 SP1	1.61	10809146
10.1 SP1	1.60	—
10.1 SP1	1.56	10808195
10.1 SP1	1.54	10803258
10.1 SP1	1.53	10789101
10.1 SP1	1.52	10799484
10.1 SP1	1.48	10803632
10.1 SP1	1.47	10800229
10.1 SP1	1.45	10806600
10.1 SP1	1.44	10804701
10.1 SP1	1.43	10804693
10.1 SP1	1.42	10804838
10.1 SP1	1.41	10802379
10.1 SP1	1.38	10804156
10.1 SP1	1.37	10804054
10.1 SP1	1.35	10804054
10.1 SP1	1.31	10804071
10.1 SP1	1.29	10801777
10.1 SP1	1.28	—
10.1 SP1	1.27	10795138
10.1 SP1	1.26	10801214
10.1 SP1	1.25	10797670
10.1 SP1	1.24	10796798
10.1 SP1	1.22	10796595
10.1 SP1	1.21	10800274
10.1 SP1	1.19	10798592
10.1 SP1	1.18	10796718
10.1 SP1	1.17	10799155

Quartus II Software Version	Patch	Customer Service Request Number
10.1 SP1	1.16	10798840
10.1 SP1	1.15	10790891
10.1 SP1	1.14	10784605
10.1 SP1	1.13	10796556
10.1 SP1	1.12	10790750
10.1 SP1	1.10	10795756
10.1 SP1	1.09	10794997
10.1 SP1	1.07	10797744
10.1 SP1	1.05	10794318
10.1 SP1	1.03	10791214
10.1	0.73	10809631
10.1	0.71	10803647
10.1	0.70	10797641
10.1	0.68	—
10.1	0.67	10792431
10.1	0.66	10802357
10.1	0.64	10796798
10.1	0.63	10796584
10.1	0.62	10800492
10.1	0.61	10795138
10.1	0.60	10799343
10.1	0.57	10798840
10.1	0.56	10793065
10.1	0.52	10796584
10.1	0.50	10795119
10.1	0.49	10796732
10.1	0.48	10762591, 10796158
10.1	0.45	10780326
10.1	0.44	10792657
10.1	0.42	10794218
10.1	0.40	10793494
10.1	0.39	10786693

Quartus II Software Version	Patch	Customer Service Request Number
10.1	0.38	10791183
10.1	0.36	10791214
10.1	0.35	10753942
10.1	0.32	10784605
10.1	0.30	10790750
10.1	0.22	10785030
10.0 SP1	1.213	10808740
10.0 SP1	1.211	10803647
10.0 SP1	1.208	10799492
10.0 SP1	1.198	10785300
10.0 SP1	1.194	10788543
10.0 SP1	1.187	—
10.0 SP1	1.185	10784253
10.0 SP1	1.180	10775162
10.0 SP1	1.170	10781078
10.0 SP1	1.169	10779281
10.0	0.62	—
10.0	0.34	10758918
9.1 SP2	2.71	10758718
9.1 SP2	2.70	10757551
9.1 SP2	2.130	10807251
9.1 SP2	2.129	10789946
9.1 SP2	2.09	10751053
9.1	0.97	10789946

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
May 2011	1.0	Initial release.